

nanoHUB: Use of External Resources by External Researchers

Research Article

Analysis of CNT Bundle and Its Comparison with Copper Interconnect for CMOS and CNFET Drivers

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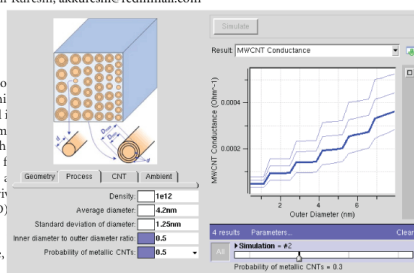
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In nanoscale regime as the CMOS process technology is approaching 32 nm, a major hurdle for on-chip communication due to high resistance of metal interconnects and in nanoscale-integrated circuits. The performance of metal interconnect (CNFET) as a driver and compared with HSPICE simulations are carried out at operating frequency of 1 GHz. The CNFET driver can potentially provide a delay of 1.5 ns with 32 nm process technology. Similarly, the CNFET driver can provide a delay of 1.5 ns with traditional interconnect at all supply voltages (VDD).

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The analysis of our external literature citations revealed some examples where external theory-driven researchers utilized a nanoHUB tool that has been contributed to nanoHUB from outside of the NCN. For example the authors Kureshi and Hasan working at a university in India published their study CNT bundles as possible copper replacement interconnects in the “Journal of Nanomaterials” in April 2009. In their work they utilized the tool “Carbon Nanotubes Interconnect Analyzer (CNIA)” for over 1,600 simulations in the year 2009 alone. CNIA was contributed by Tanachutiwat and Wang of the University of Albany. We cannot see any relationship between the two research groups and NCN other than the contributed, efficiently served, and utilized tool CNIA. The same CNIA tool has previously also been cited in a Master’s thesis at the University of Cincinnati in 27 the year 2005. The concept of community contributions coming from outside the NCN and being useful for an unrelated research group is becoming reality.