**Test for MOSCap Lab**

(<http://nanohub.org/resources/moscap>)

Note: only one choice is correct

1. What direction should gate bias (Vg) be applied to push a p-type doped Si MOS-Capacitor structure into inversion?
   1. Increasing Vg
   2. Decreasing Vg
   3. Vg=0 V
2. Which one would be a suitable mid-gap work function material for Si channel device?
   1. Al: 4.2eV
   2. Mo: 5.45eV
   3. Ni: 5.04eV

Figure 1

1. Figure 1 represents a C-V obtained from a MOS structure. What is true about the apparatus?
   1. N-type substrate and High frequency measurement
   2. N-type substrate and Low frequency measurement
   3. P-type substrate and Low frequency measurement
2. In what mode is the MOS in during X in Figure 1?
   1. Accumulation
   2. Inversion
   3. Depletion
3. Which point is closest to threshold voltage (Vt) point, i.e. VG ~=Vt?
   1. X
   2. Y
   3. Z
4. What is thickness of inversion layer?
   1. ~ 1 µm
   2. ~ 2 nm
   3. ~ 0.1 µm
5. Which type of device does not have a MOS like structure?
   1. Charged coupled devices (CCD)
   2. High electron mobility transistor (HEMT)
   3. Gate all around nanowire (GAA NW) transistor
6. How would a high frequency C-V characteristics look like when the substrate is heavily doped?
7. What is the standard frequency at which C-V measurement are experimentally done?
   1. 1 Hz
   2. 1 MHz
   3. 1 GHz
8. The gate material in a MOS structure is designed using a p-type Si doped at the level of 1018 /cm3.What is the shift in threshold voltage |ΔVt| if doping is erroneously done at 1019 /cm3.
   1. 0.535 V
   2. 0.0595 V
   3. 0.476 V
9. A high frequency C-V characteristic of a MOS-C structure (blue) is as shown in the figure below. How would the new C-V characteristic (red) look like if oxide material is replaced with a high-k material of same thickness.
10. What is the cause of interfacial traps?
    1. Dangling bonds at Si surface
    2. Sodium Ions (Na+)
    3. Trapped electrons
11. What is the ideal surface trap density after annealing steps?
    1. <1013 /cm2-eV
    2. <1012 /cm2-eV
    3. <1010 /cm2-eV
12. C-V characteristic of a P channel MOS is shown in figure below. What is the threshold voltage of the device?

* 1. 2 V
  2. -1 V
  3. 0 V

1. What operation will shift the threshold voltage to 0V?
   1. Increase oxide thickness
   2. Increase channel doping
   3. Increase gate work function