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Interfacial Trap Effects in InAs Gate-all-around Nanowire Tunnel Field-Effect Transistors: First-Principles-Based Approach

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- Motivation
 - Single defect effect
- Simulation approach
 - DFT defect modeling / NEGF
- Simultaion result
 - L_G scaling / x_T variation
- Conclusions

Potential of TFET Motivation



- Low ON-state current issue
 - Heterojunction (III-V/III-V, III-V/Si)
 - ✓ Gate-all-around nanowire (GAA NW)

E. Memsievic et al., Nano Lett., 2017

-0.5

Gate-meta

Drain space

Drain



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-0.25

0

0.25

0.5

 $5 \Delta V_{GS} = 0.1 V$

Defect-induced degradation Motivation



R. N. Sajjad et al., IEEE TED, 2016





Km. S. Singh, et al., IEEE T. Device Mat. Re., 2020

Defect has been one of the critical issue for the practical applications of TFETs

- **Trap-assisted tunneling (TAT)**
- **Electrostatic degradation by trapped charges** Low-defect fabrication process of NW → Importance of a single defect analysis on GAA **NW III-V TFET at nanoscale**



Motivation Defect models – previous works

Conventional TCAD model

- Many fitting parameters for various current mecahnisms (BTBT, TAT)
- Limit of the analysis of the impact of a single defect on NW TFET at nanoscale

Full quantum transport model for a single defect is necessary Nonequilibrium Green's function (NEGF) studies for a single defect

- $k \cdot p$ Hamiltonian + Cubic potential well (M. G. Pala, *IEEE TED*, 2013)
- Tight-binding (TB) Hamiltonian + Screened Coulomb potential (P. Long, JAP, 2018)
- TB Hamiltonian with adjusted TB parmeters (M. Rau, Ph.D. Thesis, 2019)
 - Lack of physical defect information → No linkage between specific defect types and TFET performances
 - Charge trapping effects have not been rigorously treated
 - → Physically-relevant atomic defect Hamiltonians are essential



In this work,

- Physically-relevant interfacial defects whose energy level is located in the band gap are handled by the first principles approach for InAs/Al₂O₃ GAA NW TFET
- Full quantum tranport model including electron-phonon scattering is employed to exactly capture the trap-assisted tunneling (TAT) and charge trapping in the defect states
- ✓ The impact of gate length (L_G) scaling with a single trap are closely investigated



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Method **DFT defect modeling**



- Several first-principles studies on the interfacial defects at III-V/high-k oxide have reported that dangling bond and antisite are dominant sources for bandgap defect [1], [2]
- In this work, As-dangling bond (As_{DB}) and As-antisite (As_{In}) between InAs/Al₂O₃ nanowire are considered

[1] J. Robertson et al., JAP, 2015 [2] G. G. Diniz et al., JAP, 2017



Method **DFT defect modeling**



- $InAs/Al_2O_3$ NW with 2.18 nm x 2.32 nm
- DFT in the basis of LCAO using the SIESTA package
- Exchange-correlation: GGA-PBE functional

[1] L. G. Ferreira et al., *PRB*, 2008 [2] L. Lin, *JAP*, 2013



Method **DFT defect modeling**



- Spacing between the periodic defects ≥ 11 Å to eliminate the interaction between imaginary defects [1]
- Bandgap underestimation of GGA is corrected by employing the DFT-1/2 method [2]
- Structure relaxed until maximum force < 0.05 eV/Å with 3x1x1 Monkhorst-Pack k-grids

[1] L. Lin, *JAP*, 2013 [2] L. G. Ferreira et al., *PRB*, 2008

Method Mode-space in heterostructures



- The size of DFT Hamiltonians is prohibitively large for the NEGF simulations
- Mode space method originally developed for DFT Hamiltonian [1] is extended to heterogeneous system where a single defect is introduced
 - \rightarrow Our novel method gurantees no unphysical states mentioned in [2]



Method NEGF Phonon scattering

Limit of ballistic NEGF simulation for defect study

- Defect density of states is very sharp (Dirac-like LDOS)
 → Convergence problem during self-consistent calculations between NEGF and Poisson's equations [1]
- Non-physical behavior, such as artificial negative differential resistance, may occur without inelastic scattering [2]

Electron-phonon scattering (elastic/inelastic) is included using deformation potential [3] within self-consistent Born approximation

$$\Sigma_{ac}^{\leq}(E) = \frac{D_{ac}^{2} k_{B} T}{\rho v_{s} \Omega} SG^{\leq}(E)S$$

$$\Sigma_{op}^{\leq}(E) = \frac{\hbar D_{op}^{2}}{2\rho \omega \Omega} S\left(n_{\omega} G^{\leq}(E + \hbar \omega) + (n_{\omega} + 1)G^{\leq}(E - \hbar \omega)\right)S$$

 $D_{ac/op}$: acoustic/optical deformation potentials

[1] thesis, Rau, 2019[2] M. Bescond, JAP, 2010[3] C. Klinkert, ACS Nano, 2020



Simulation setup / parameters **Method**



ħω : 30 meV

Gate length (L_G) scaling simulation

L_G is varied from 7 nm to 17 nm Defect is asummed to be located in the middle of the channel

Defect location (x_{τ}) simulation x_{T} is varied from -6 nm to 6 nm Drain-side defect ($x_{T} < 0$) Source-side defect ($x_T > 0$) L_G is set to be 17 nm

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Supercell band structures



Supercell size Defect-free : 1012 atoms As_{In} : 1013 atoms As_{DB} : 1012 atoms

Both types of the defect are demonstrated to be sources for the bandgap states $\rightarrow As_{In}$ (deep trap) / As_{DB} (shallow trap) Fermi level for each case is higher than the defect level \rightarrow Positive charges are trapped in the defect states at nonequilibrium simulations

Results

Results Local density of states of the defect states



Defect LDOS largely spreads over the first nearest neighbor (1-NN) and the second nearest neighbor (2-NN) As atoms

 $As_{In} \rightarrow 1$ -NN: 4 atoms, 2-NN: 6 atoms $As_{DB} \rightarrow 1$ -NN: 3 atoms, 2-NN: 3 atoms

1-NN atoms → 4.3 Å from the interface
2-NN atoms → 7.4 Å from the interface
→ Trapped charges in the interfacial defect permeate inside the NW

○ H ● O © As 🔘 Al 🔘 In

These atomic properties of the defects can importantly affect the electrostatics of the TFET at nanoscale, influencing TFET performance





The defect states are within tunneling window → TAT leakage current Deep/shallow properties agree with that of the results of DFT calculation However, 1) the valence band is deformed compared with the defect-free 2) Defect level of As_{In} is significantly shifted down: 0.7 eV → 0.3 eV



Results Density-averaged potential



- φ_{avg} is locally pulled down near the defect cell
 → Positive hole carriers are trapped in the defect states
- The effect of the trapped charges is more significant in As_{In} than As_{DB}
- For As_{In} , ϕ_{avg} at the defect cell is almost unchanged
 - → Trapped charges considerably screen the gate field

Results Impact of As_{In}



Impact of As_{In}

Effect 1:

Trapped charges \rightarrow push down valence band edge \rightarrow BTBT $\downarrow \rightarrow I_{DS} \downarrow$ Effect 2:

Trapped charges → strong screening
→ TAT path effectively pinned at drain Fermi
→ leakage current floor (TAT current almost constant)

For $L_G = 17$ nm, TAT is negligible due to relatively long LG \rightarrow Effect 1 dominant

Effect 1, 2 becomes severe with decreasing L_G

Results Impact of As_{DB}



Impact of As_{DB}

Effect 1:

Negligible trapped charges \rightarrow TAT states easily controlled by V_{GS} \rightarrow TAT increased with V_{GS}

Effect 2:

AsDB deforms valence band structures \rightarrow BTBT \downarrow

Results Impact of a defect on L_G scaling



The detrimental defect depends on L_G scaling range

- Deep L_G scaling (L_G < 12 nm) : As_{DB}
- Moderate L_G scaling (L_G > 12 nm) : As_{In}



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- We investigated the impacts of single interfacial defects that creates bandgap states, As_{In} and As_{DB}, on InAs GAA NW TFET at nanoscale
- The atomic properties of individual defects are rigorously investigated employing the DFT defect Hamiltonians
 → Charge trapping at interfacial defects can permeate inside the NW, not negligible for the nanoscale device
- Critical defect limiting scaling depends on L_G range

