Introduction to FETToy Simulator

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Introduction to FETToy

Description of the FETToy Simulator

- Computes ballistic I-V characteristics for:
  - Conventional MOSFETs – single or double gate
  - Nanowire MOSFETs – cylindrical geometry
  - Carbon Nanotube (CNT) MOSFETS – cylindrical geometry

A. Rahman, J. Guo, S. Datta, and M. Lundstrom, "Theory of Ballistic Nanotransistors," IEEE Trans. on Electron Devices, 50, p. 1853, 2003

Introduction to FETToy

Description of the FETToy Examples

- Example 1: Role of Gate Oxide Thickness on MOSFET characteristics
- Example 2: Role of Carrier Effective Mass on MOSFET characteristics
- Example 3: New Channel Materials
- Example 4: Two-dimensional Electrostatics
- Example 5: Compare p-type and n-type MOSFETs
- Example 6: Figures of Merit for MOSFETs
- Example 7: Figures of Merit for Nanowire MOSFETs

Problem 1

Traditional MOSFET models tell us that ID α Cox, so reducing the oxide thickness by a factor of two doubles the current. Let's see what happens for nanotransistors.

1) Explore the role of gate oxide thickness on the on-current of a ballistic silicon MOSFET. For these calculations, you should use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) and vary the oxide thickness from **10nm** to the unphysically small value of **0.01nm**. Assume *VDD* = 1V and room temperature operation.

1a) Produce a plot of the on-current (the current for *VG* = *VD* = *VDD*) vs. oxide thickness. Compare the computed results to the result expected from conventional MOSFET theory (*ID* ~ *COX*) by appropriately plotting the actual result and the trend expected from traditional theory.

1b) Provide a physical explanation for the shape of your plot. The characteristic should change when the oxide thickness is smaller than a certain value. Can you give a simple equation to estimate that value? (HINT: It is the gate capacitance that matters. The oxide capacitance is in series with a semiconductor or "quantum" capacitance)

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

1a) Conventional Plot: I_{ON} vs. T_{OX}

Common Material Parameters and Settings:

T_{OX} = 10nm **I_{D0} = ?**

Device | Models | Environment

Model: MOSFET

Single Gate/Double Gate: Single Gate

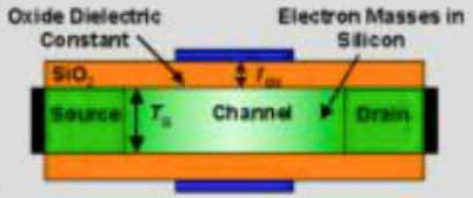
Transport Effective Mass: 0.19

Valley Degeneracy: 2

Floating Boundary Flag: no

Body Thickness: 10nm

Source Doping Density: 1.0e20/cm3



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Device | Models | Environment

Gate Insulator Thickness: 10nm

Insulator Dielectric Constant: 3.9

Threshold Voltage: 0.32V

Gate Control Parameter: 1

Drain Control Parameter: 0

Series Resistance (ohm-um): 0

Refresh Screen | Copy/Paste with Desktop

Device | Models | Environment

Ambient Temperature: 300K

Initial Gate Voltage: 0V

Final Gate Voltage: 2V

Number of Gate Voltage Bias Points: 13

Initial Drain Voltage: 0V

Final Drain Voltage: 1V

Number of Drain Voltage Bias Points: 30

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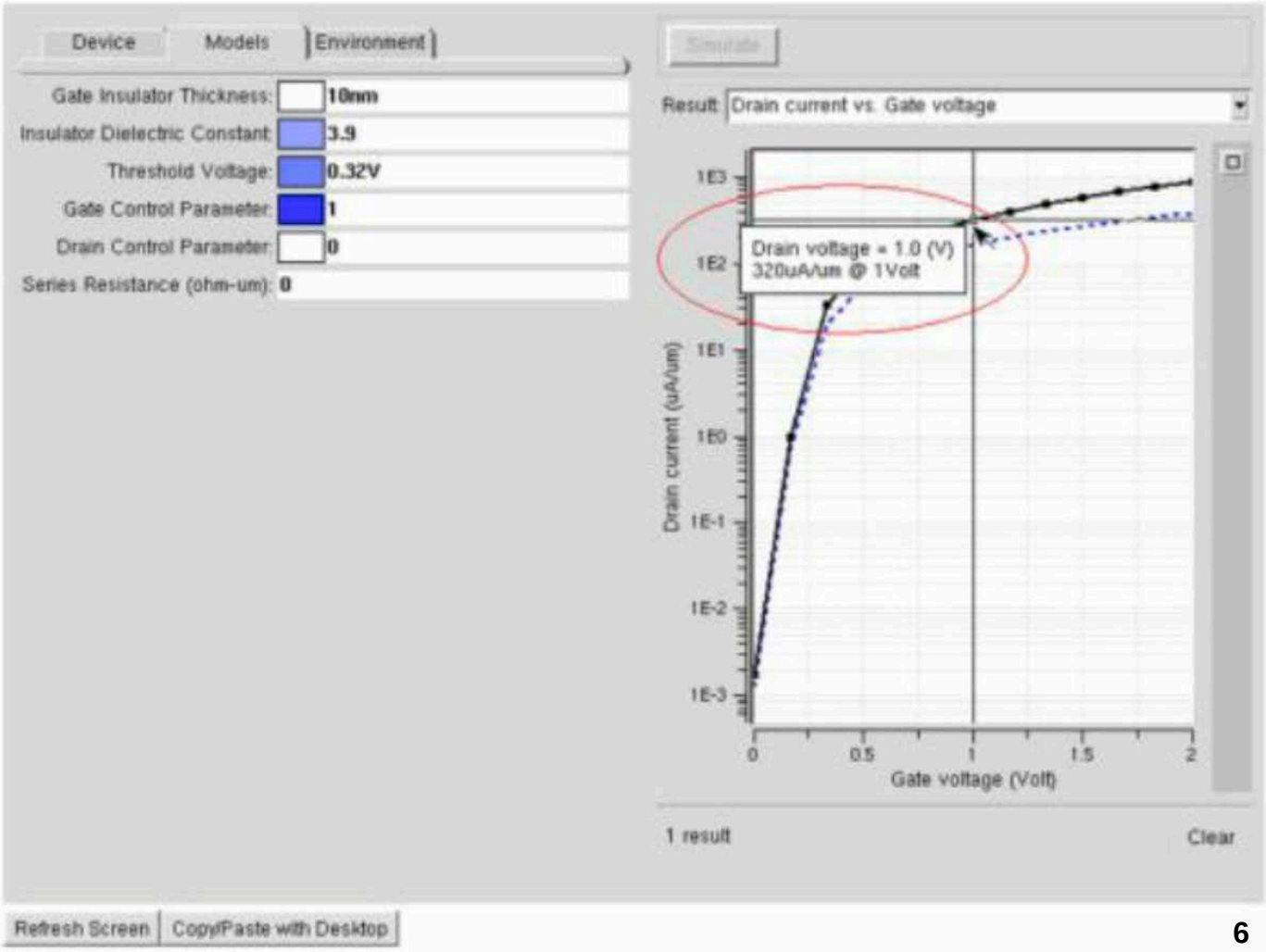
1a) Conventional Plot: I_{ON} vs. T_{OX}

Result for ID0:

T_{OX} = 10nm **I_{D0}=320uA/um**



1a) Conventional Plot: I_{ON} vs. T_{OX}

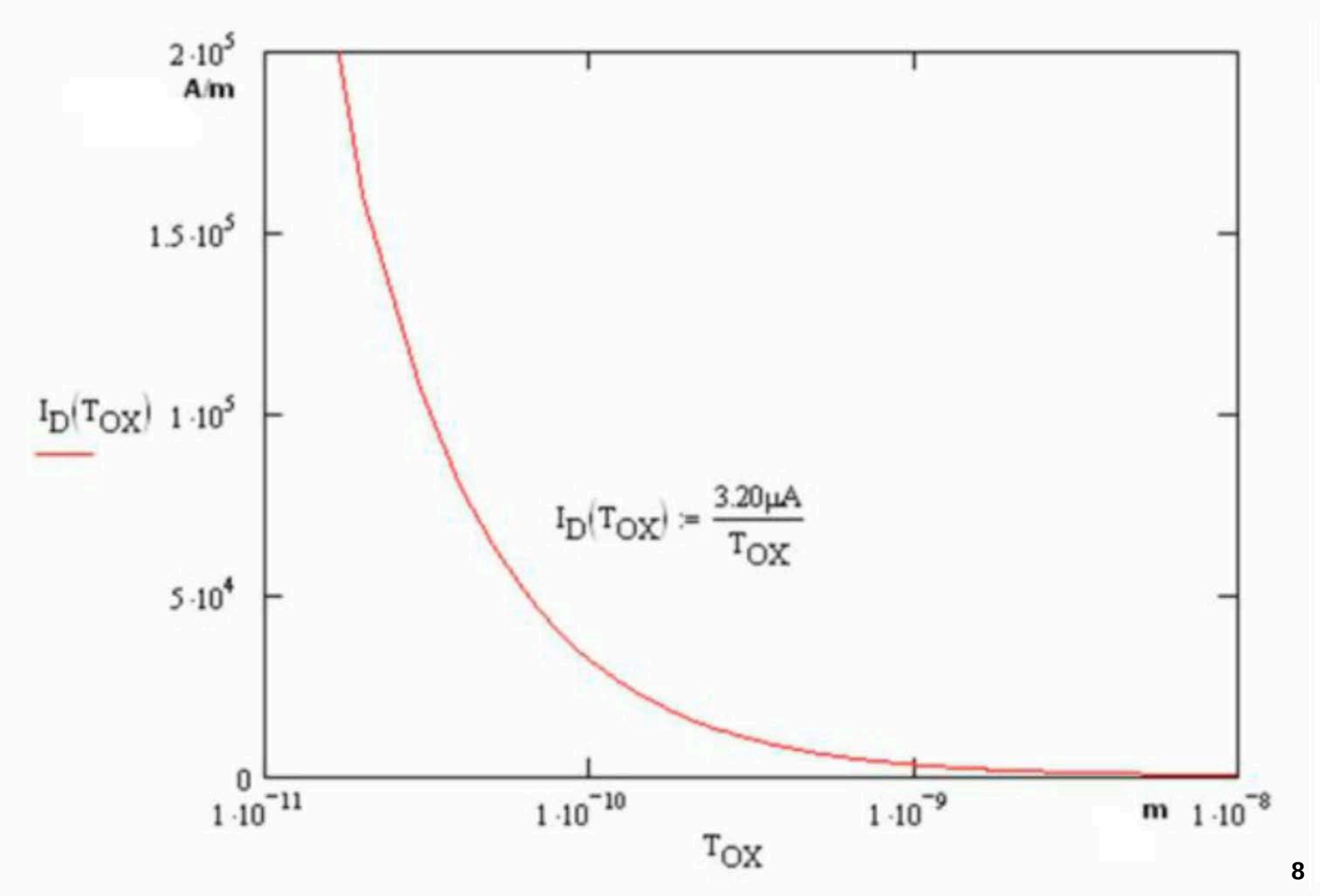
$$I_D \sim C_{OX}$$

$$I_D \sim \varepsilon_{OX}/T_{OX}$$

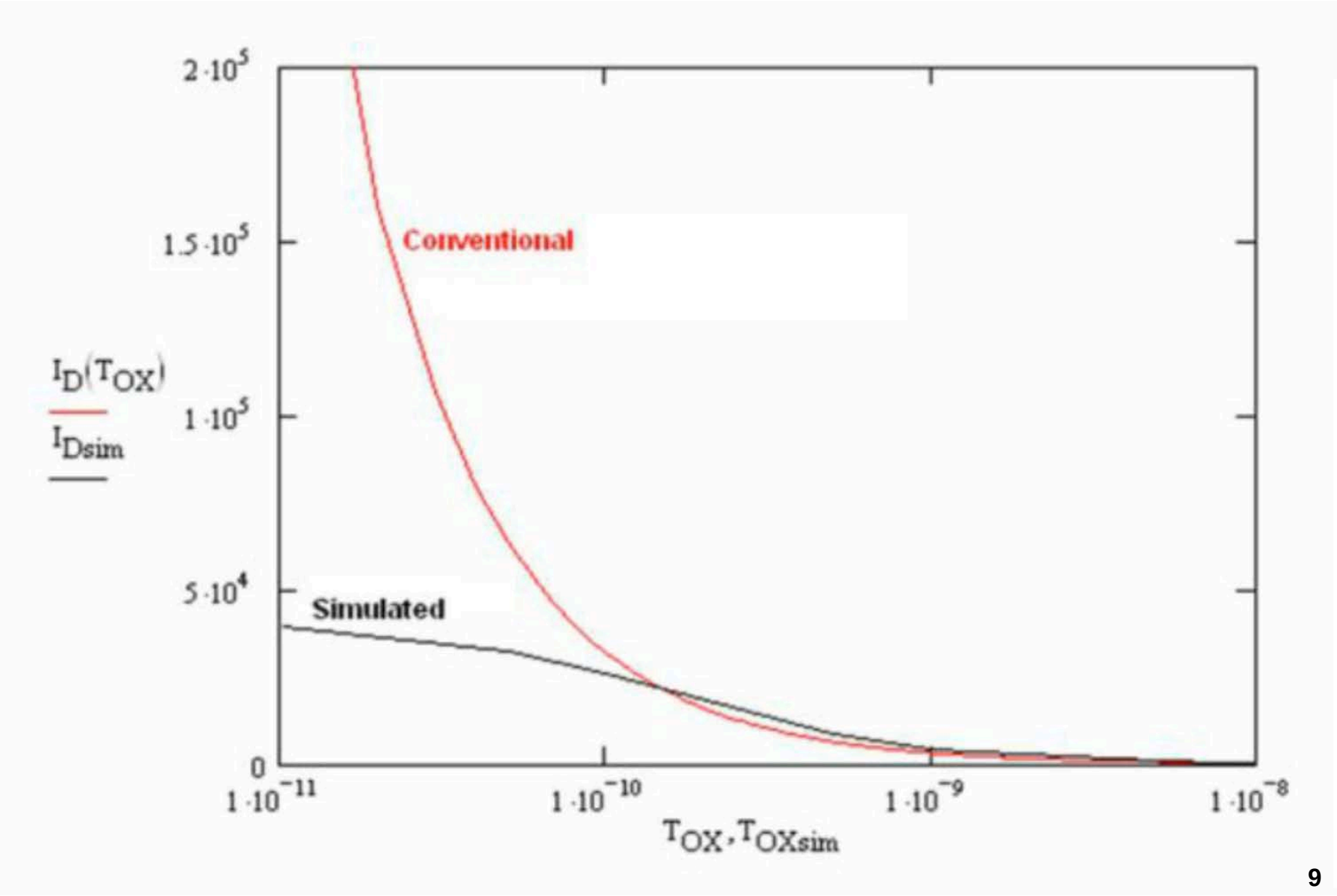
$$I_D \sim 1/T_{OX}$$

$$I_D = 320uA/um*(10nm/T_{OX})$$

1a) Conventional Plot: I_{ON} vs. T_{OX}



1a) Simulated Plot: I_{ON} vs. T_{OX}



1b) Conventional vs. Simulated

Conventional Theory:

$I_D \sim C_{OX}$

FETToy:

$I_D \sim C_G = C_{OX}C_Q/(C_{OX}+C_Q)$

$C_G \rightarrow C_{OX}$ if $C_Q >> C_{OX}$ (Conventional holds)

$C_G = C_{OX}C_Q/(C_{OX}+C_Q)$ otherwise (Conventional fails)

Decreasing $T_{OX} \rightarrow$ Increasing $C_{OX} \rightarrow$ Failure of $C_Q >> C_{OX}$ condition

$C_Q = q^2D = q^{2*}2m_{eff}/(\pi h_{bar}) = 2.54E\text{-}5F/cm^2$

$C_{OX} >> C_Q$ (Conventional holds)

Fails when: $C_{OX} = C_Q$

$C_{OX} = C_Q$

$\varepsilon_{OX}/T_{OX} = C_Q$

$T_{OX} = \varepsilon_{OX}/C_Q$

$\underline{T_{OX} = .136nm}$

Problem 2

One might think that a lighter effective mass would give a transistor higher current, because with a lighter mass, carriers travel faster. This exercise will demonstrate that this is not always the case.

2) Explore the role of effective mass on the on-current of a ballistic silicon MOSFET. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) and vary the effective mass from **10m0** to **0.01m0**. Assume *VDD* = 1V and room temperature operation.

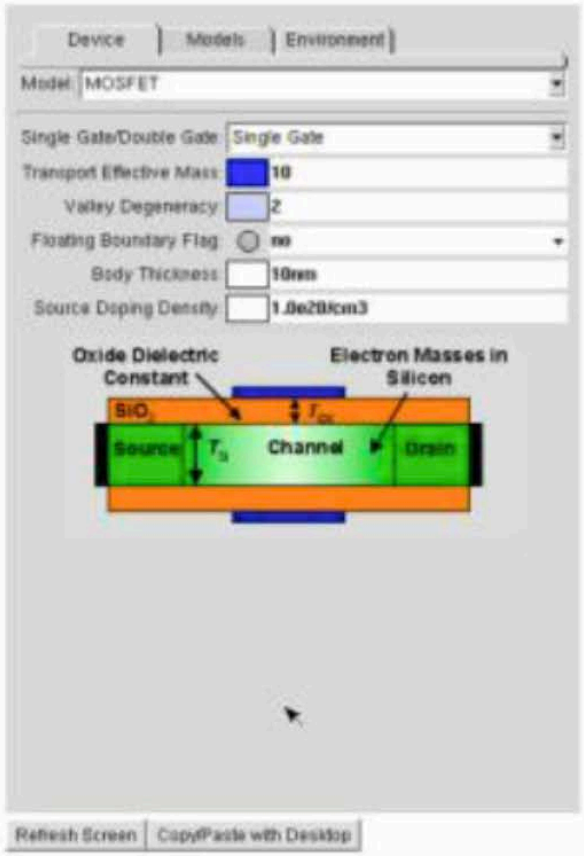
2a) Produce a plot of the on-current (the current for *VG* = *VD* = *VDD*) vs. effective mass. You might expect the on-current to be proportional to the velocity (which is inversely proportional to the square root of the effective mass). Compare your plot against this expectation by appropriately plotting the results.

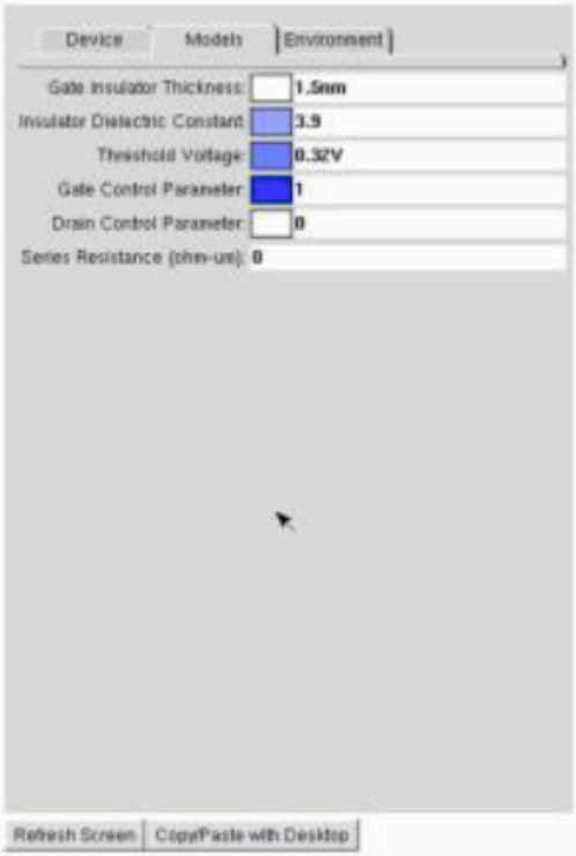
2b) Provide a physical explanation for the shape of your plot. That is, explain why the plot of *ID*(on) vs. m^* has a maximum. Hint: consider the influence of the quantum capacitance.

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

2a) Conventional Plot: I_{ON} vs. m_{eff}

Common Material Parameters and Settings:
$m_{eff} = 10m_0$ I_{D0}=??

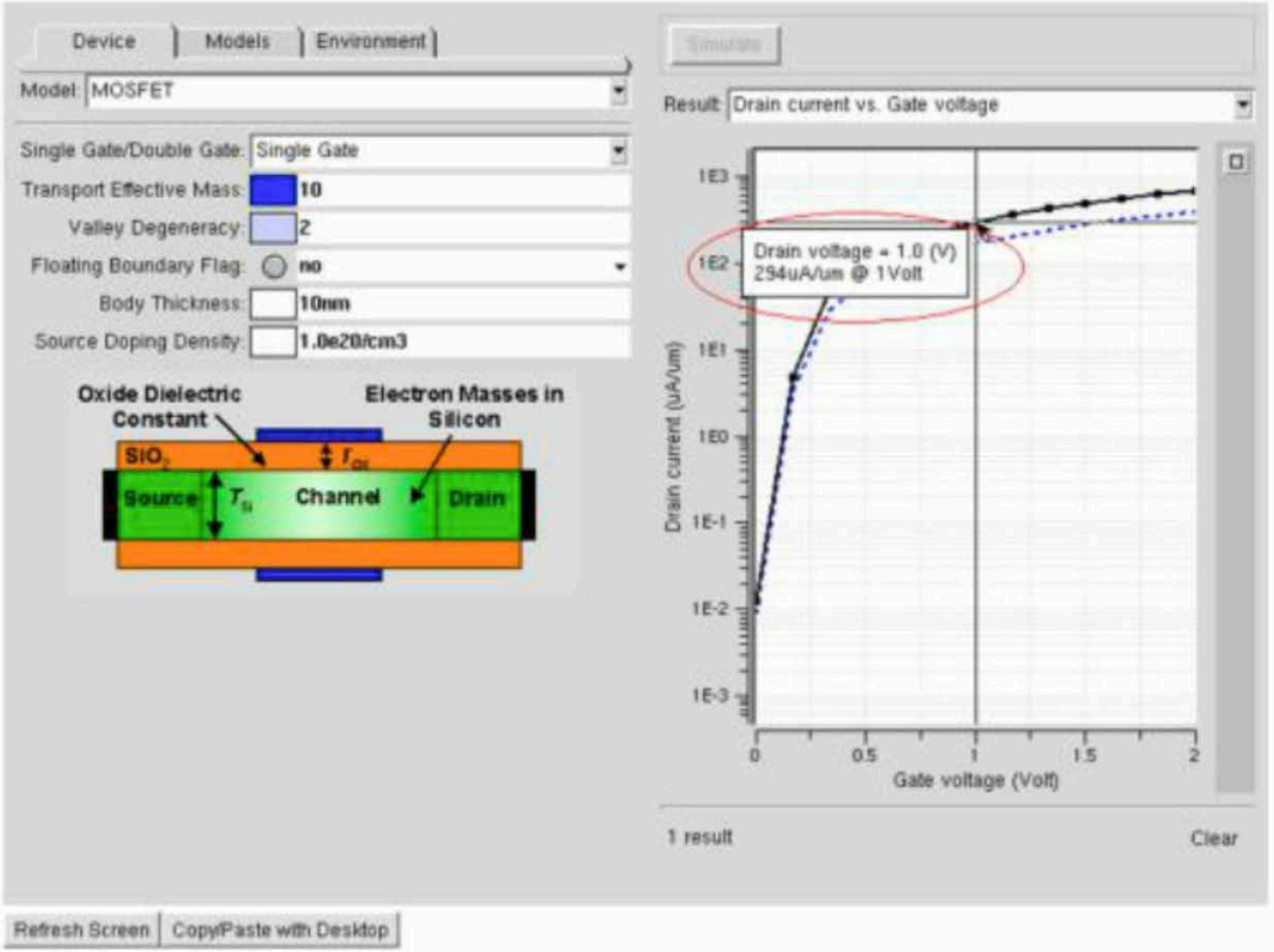




2a) Conventional Plot: I_{ON} vs. m_{eff}

Result for ID0:

$m_{eff} = 10m_0$ **I_{D0}=294uA/um**



2a) Conventional Plot: I_{ON} vs. m_{eff}

$$I_D = Q \cdot v$$

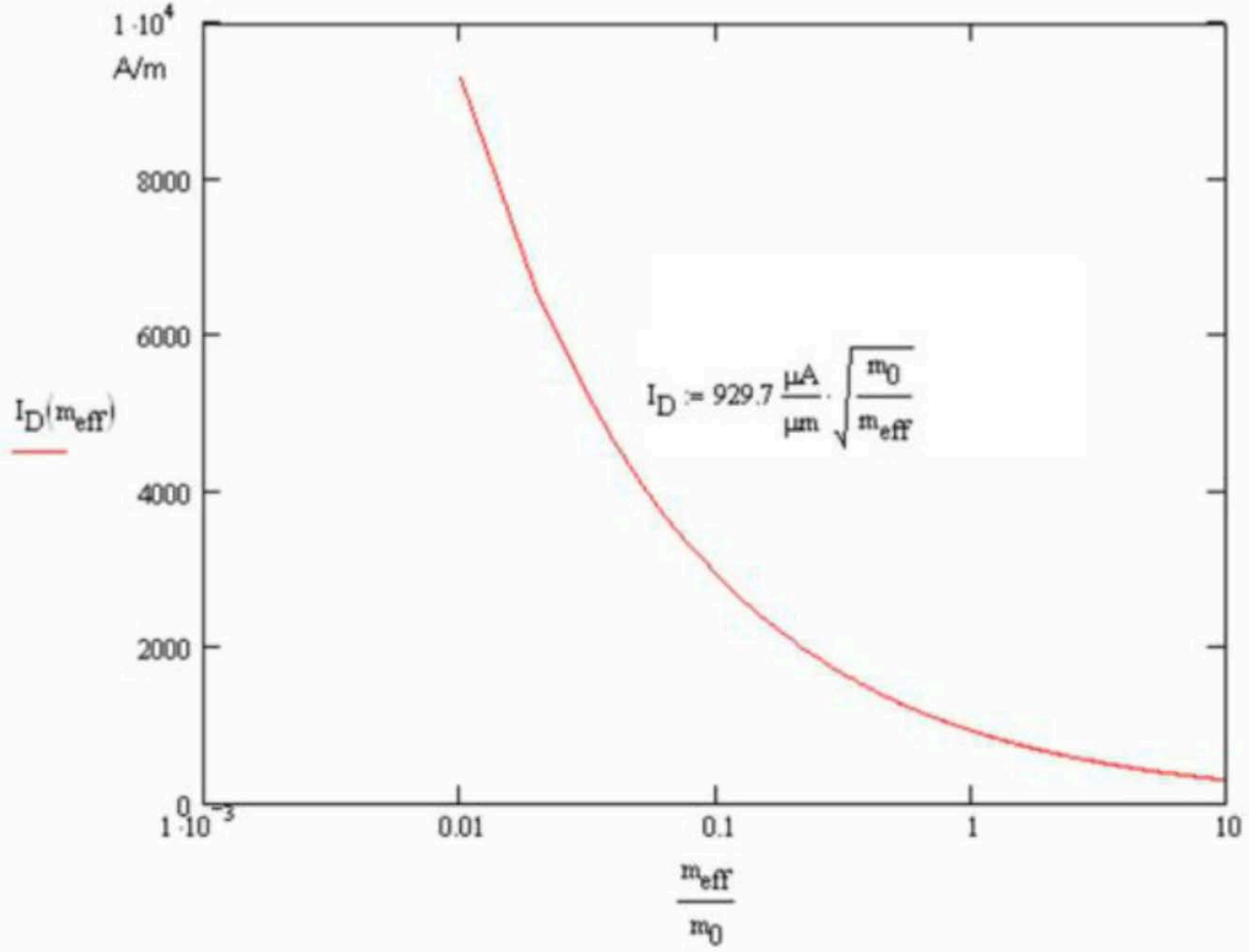
$$v \sim \frac{1}{\sqrt{m_{eff}}}$$

$$I_D \sim \frac{1}{\sqrt{m_{eff}}}$$

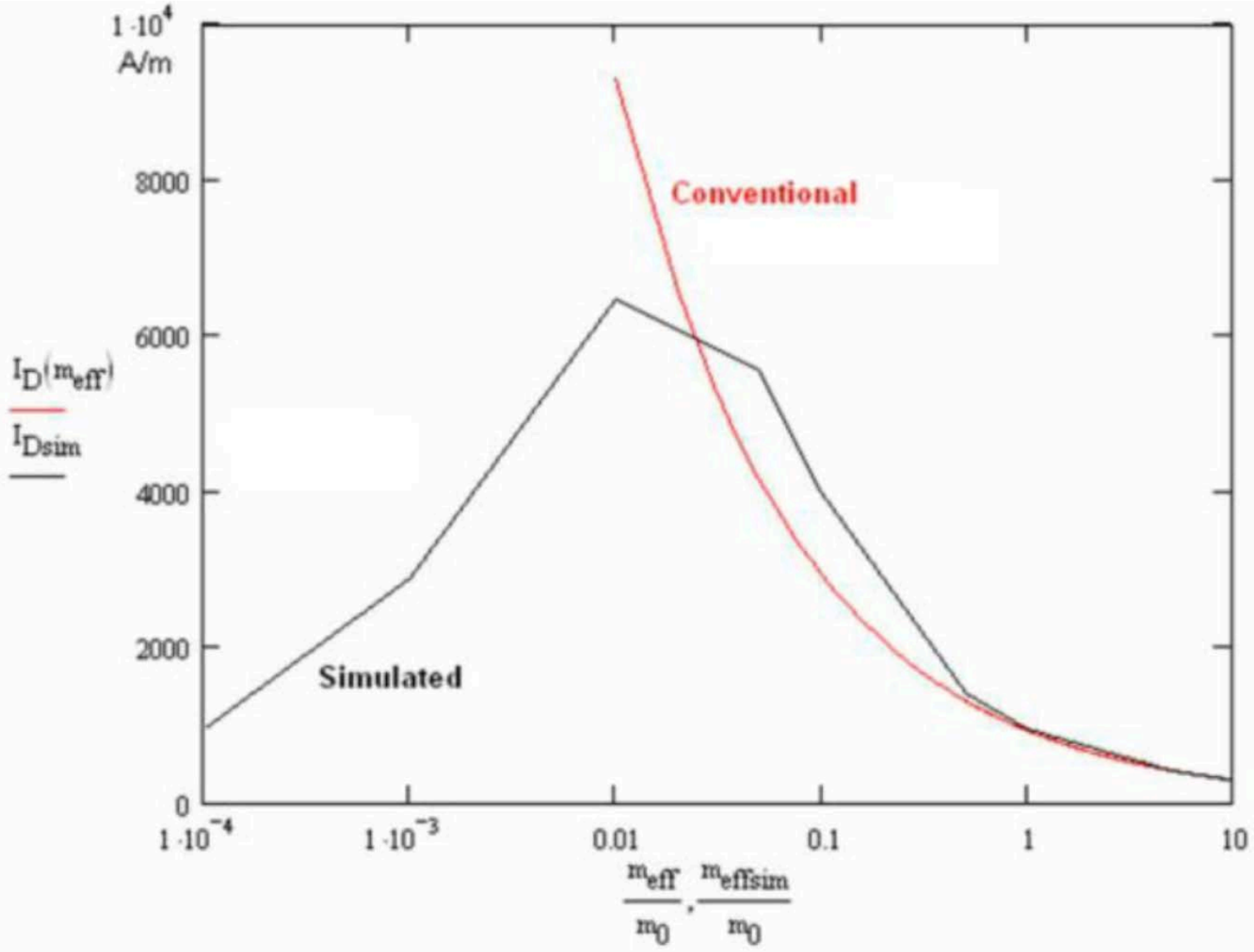
$$I_D = \frac{8.874 \cdot 10^{-13} \frac{\mu A}{\mu m} \cdot \sqrt{kg}}{\sqrt{m_{eff}}}$$

$$I_D = 929.7 \frac{\mu A}{\mu m} \cdot \sqrt{\frac{m_0}{m_{eff}}}$$

2a) Conventional Plot: I_{ON} vs. m_{eff}



2a) Conventional vs. Simulated



2b) Conventional vs. Simulated

Recall:

$I_D = Q^* v_{inj}$ where $Q = C_G(V_G - V_T)$

Conventional Theory:

$C_G = C_{OX}$

FETToy:

$C_G = C_{OX}C_Q/(C_{OX}+C_Q)$ where $C_Q = 2^*q^{2*}m_{eff}/(\pi^*h_{bar}^2)$ ➔ $C_Q \sim m_{eff}$

$C_G \rightarrow C_{OX}$ if $C_Q >> C_{OX}$ (conventional holds)

Decrease m_{eff} → failure of $C_Q >> C_{OX}$ condition → Decrease C_G

$I_D = C_G(V_G - V_T)v_{inj}$ Decrease C_G → Decrease I_D

2b) Conventional vs. Simulated

Further decreasing m_{eff}:

Decreasing m_{eff} will eventually lead to $C_Q << C_{OX}$ ➔ $C_G \rightarrow C_Q$

$$I_D = C_Q * (V_G - V_T) * v_{inj}$$

$$I_D \sim m_{eff} * v_{inj}$$

$$I_D \sim m_{eff} / \sqrt{m_{eff}}$$

$$I_D \sim \sqrt{m_{eff}}$$

Conclusion:

$I_D \sim 1/\sqrt{m_{eff}}$ if $C_Q >> C_{OX}$

$I_D \sim \sqrt{m_{eff}}$ if $C_Q << C_{OX}$

Problem 3

There is considerable interest these days in exploring the use of alternative channel materials such as Ge, GaAs, and InAs. How much performance advantage can be expected from these "new" materials?

3) Compare the on-currents of ballistic silicon, germanium, gallium arsenide, and indium arsenide n-MOSFETs. For this calculation, you should also use ***1D electrostatics*** *(gate control parameter = 1 and drain control parameter = 0) Assume VDD = 1.0V, room temperature operation, and select the appropriate effective mass and valley degeneracies for each case.*

3a) Assume an insulator thickness of 5 nm and a dielectric constant of 3.9. Simulate the four ballistic MOSFETs and compare their on-currents.

3b) Assume an insulator thickness of 0.5 nm and a dielectric constant of 3.9. Simulate the four ballistic MOSFETs and compare their on-currents.

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

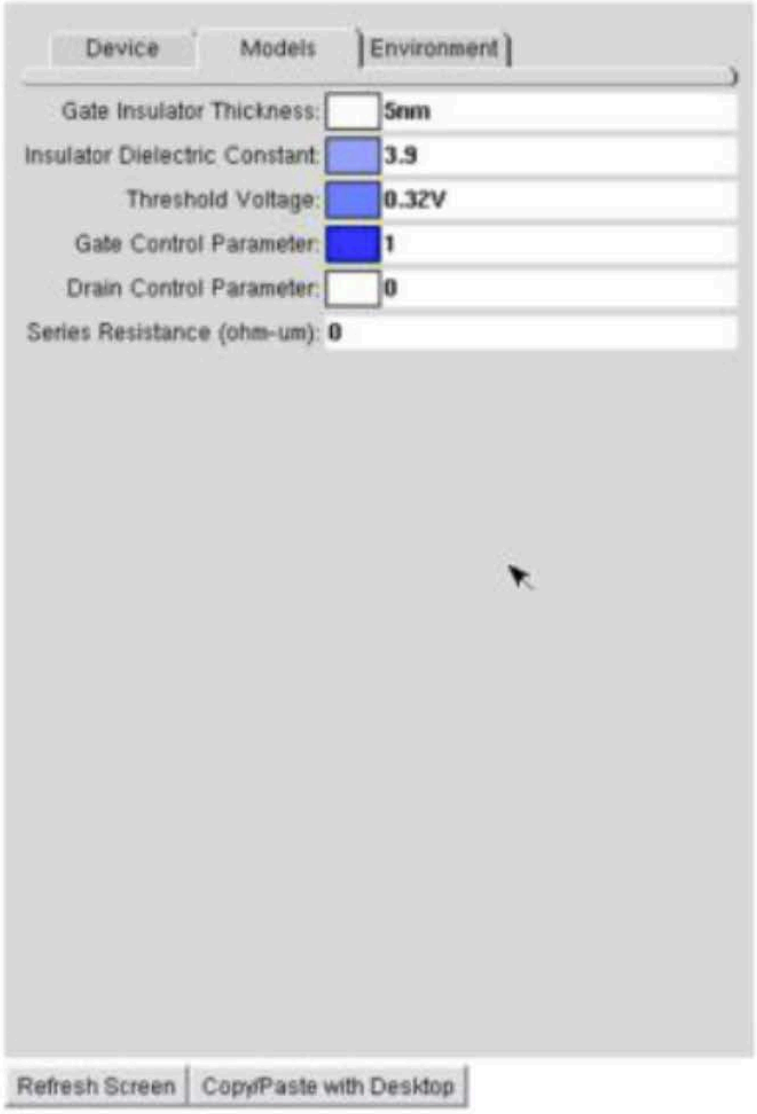
3a) On-currents with T_{OX} = 5nm

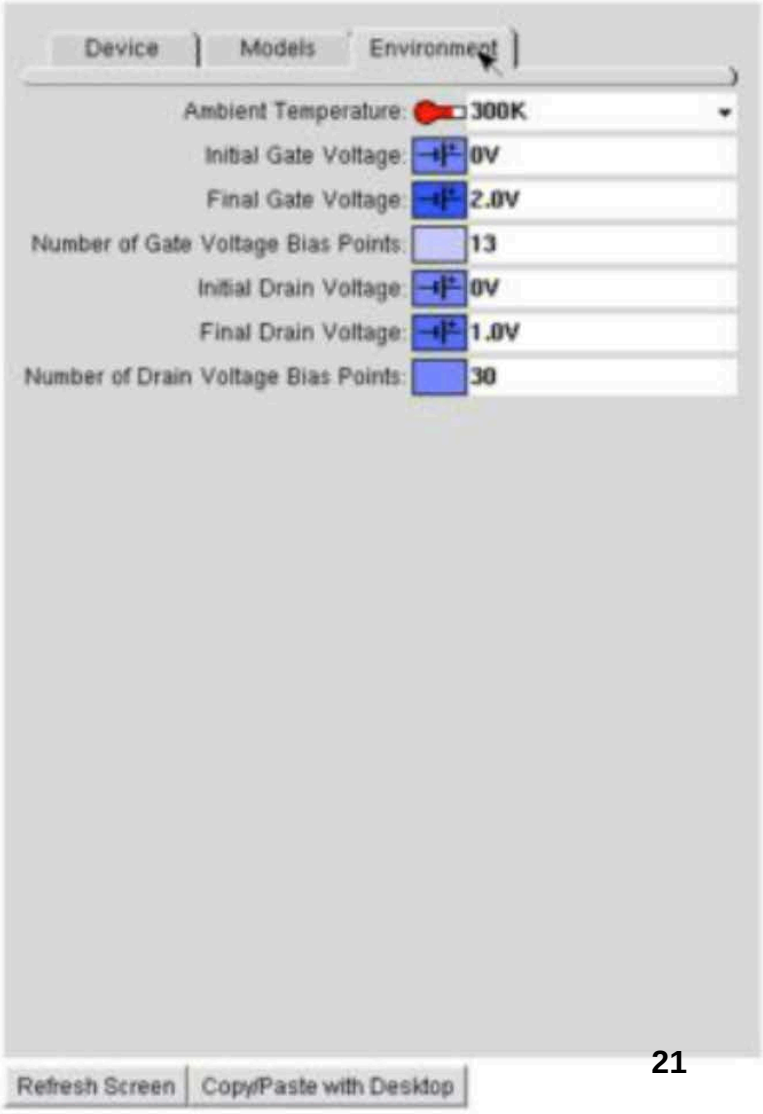
Required Material Parameters:

Material	Effective Electron Mass	Valley Degeneracy
Si	$.19m_0$	2
Ge	$.082m_0$	1
GaAs	$.067m_0$	1
InAs	$.023m_0$	1

3a) On-currents with T_{OX} = 5nm

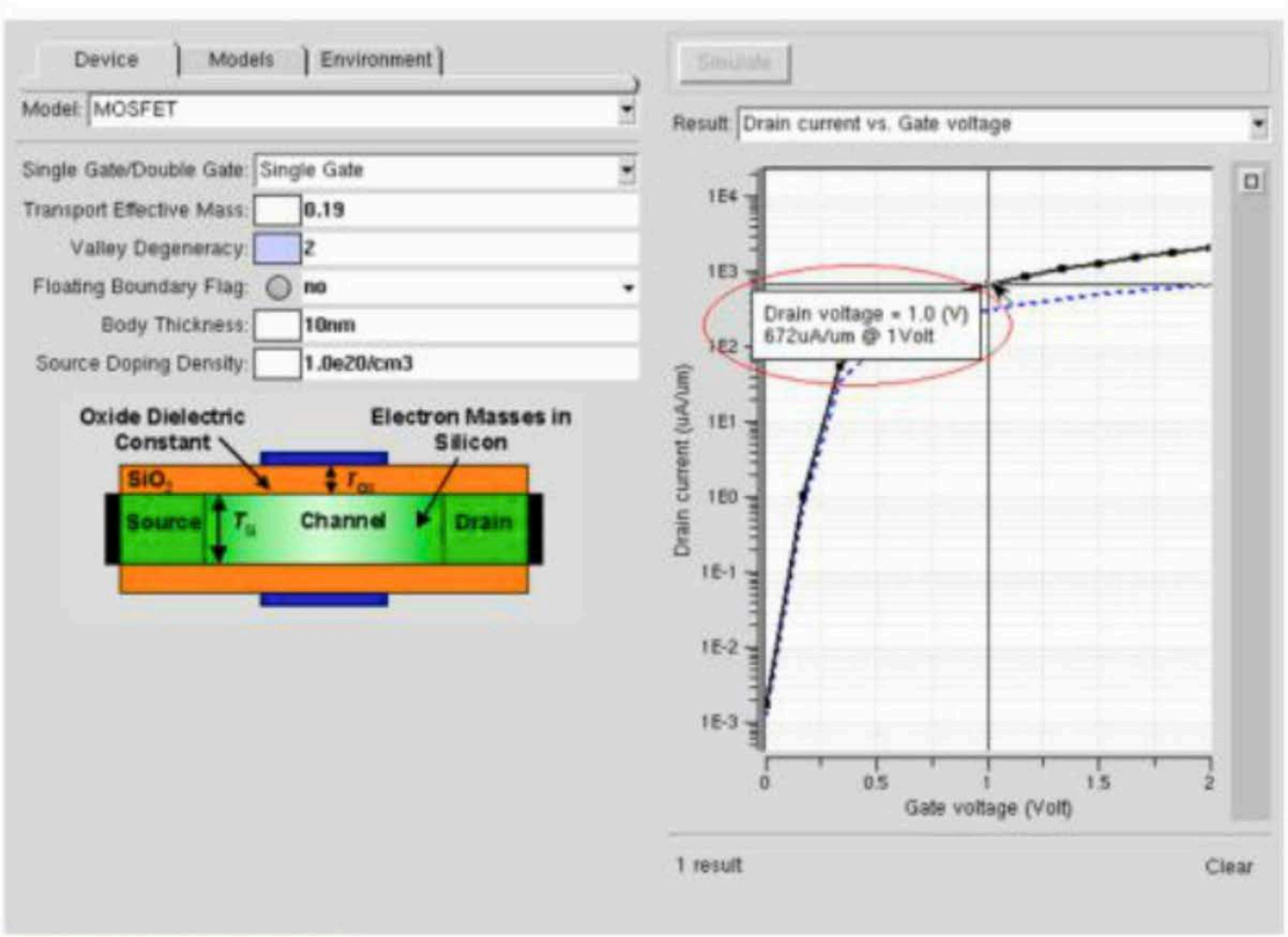
Common Material Parameters and Settings:





3a) On-currents with T_{OX} = 5nm

Material Parameters and Settings for Si,
Result for Si MOSFET: I_{ON_Si} = 672A/m



3a) On-currents with T_{OX} = 5nm

Table of Results:

Material	Effective Electron Mass	Valley Degeneracy	I_{ON}(A/m) T_{OX} = 5nm
Si	$.19m_0$	2	672
Ge	$.082m_0$	1	1270
GaAs	$.067m_0$	1	1450
InAs	$.023m_0$	1	2350

3b) On-currents with T_{OX} = .5nm

Table of Results:

Material	Effective Electron Mass	Valley Degeneracy	I_{ON}(A/m) T_{OX} = 5nm	I_{ON}(A/m) T_{OX} = .5nm
Si	$.19m_0$	2	672	8730
Ge	$.082m_0$	1	1270	8230
GaAs	$.067m_0$	1	1450	8060
InAs	$.023m_0$	1	2350	6140

3c) Comparison: 5nm vs. 0.5nm

T_{OX} = 5nm

Decreasing m_{eff} → Increasing I_{ON}

Implies: $C_Q >> C_{OX}$ or $C_Q \approx C_{OX}$

$C_Q \sim m_{eff}$

For InAs with T_{OX} = 5nm

C_Q:

$$C_Q = q^2 m_{eff}/(\pi * h_{bar}^2) * n_v$$

$$C_Q = 1.54E\text{-}6F/cm^2$$

C_{OX}:

$$C_{OX} = \varepsilon_{OX}/T_{OX} = 3.9\varepsilon_0/T_{OX}$$

$$C_{OX} = 6.91E\text{-}7F/cm^2$$

Conclusion:

$$C_Q > C_{OX}$$

At conventional limit, CG ≈ COX

$$I_D = Q * v \sim 1/\sqrt{m_{eff}}$$

3c) Comparison: 5nm vs. 0.5nm

T_{OX} = 0.5nm

Decreasing m_{eff} → Decreasing I_{ON}

Implies: $C_Q << C_{OX}$

For InAs with T_{OX} = 0.5nm

$C_Q = 1.54E\text{-}6F/cm^2$

C_{OX}:

$C_{OX} = 6.91E\text{-}6F/cm^2$

Conclusion:

$C_{OX} >> C_Q$

At C_Q limit, $C_G << C_{OX}$

$I_D = Q^*v \sim \sqrt{m_{eff}}$

See Problem 2 Part b for more details on the relationship between C_Q and m_{eff}.

Problem 4

The on-current is commonly used as a device metric, but the entire I-V characteristic is important in a switching transient. How do the shapes of the IDS vs. VDS characteristics of different MOSFETs compare?

4) Simulate ballistic silicon, germanium, gallium arsenide, and indium arsenide n-MOSFETs using an insulator thickness of 1nm. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0) Assume VDD = 1V, room temperature operation and select the appropriate effective mass and valley degeneracies for each case. For this exercise, you only need to consider VG = VDD.

4a) Normalize each IDS vs. VDS characteristic by plotting (IDS/ION) vs. *VDS*. Plot all four results on the same set of axes and compare the shape.

4b) Discuss your results and provide a physical explanation for any difference that you observe.

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

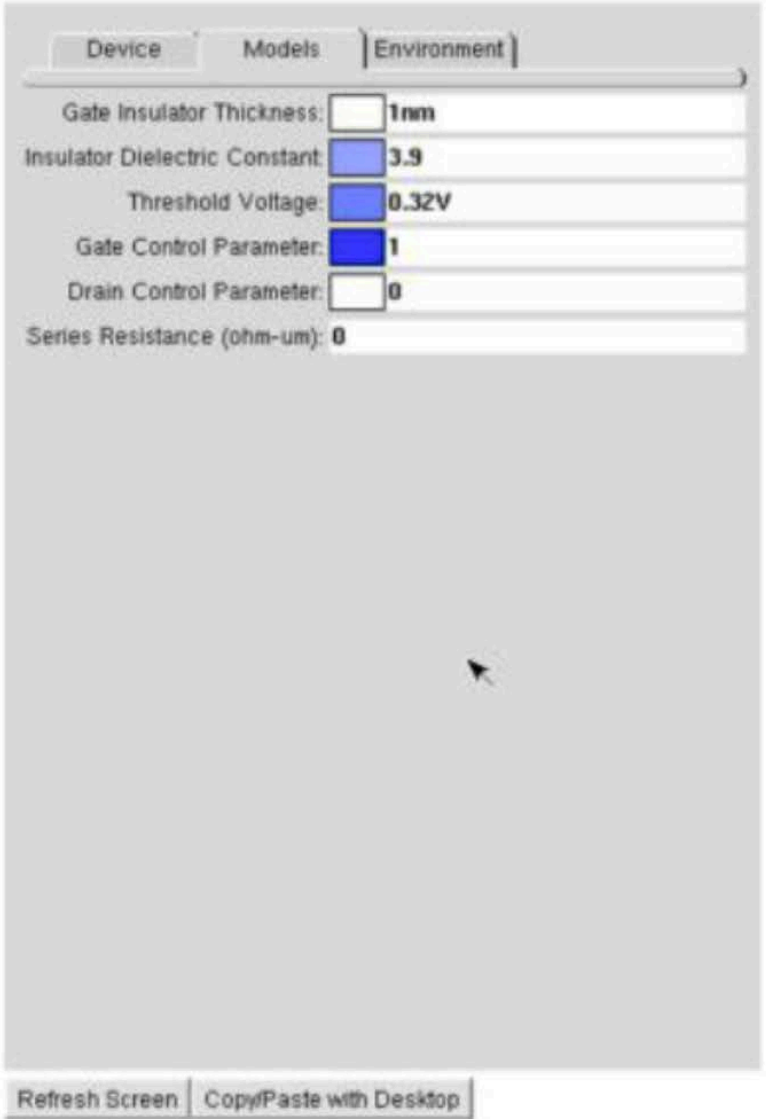
4a) Simulated Plot of I_D/I_{ON} vs. V_{DS}

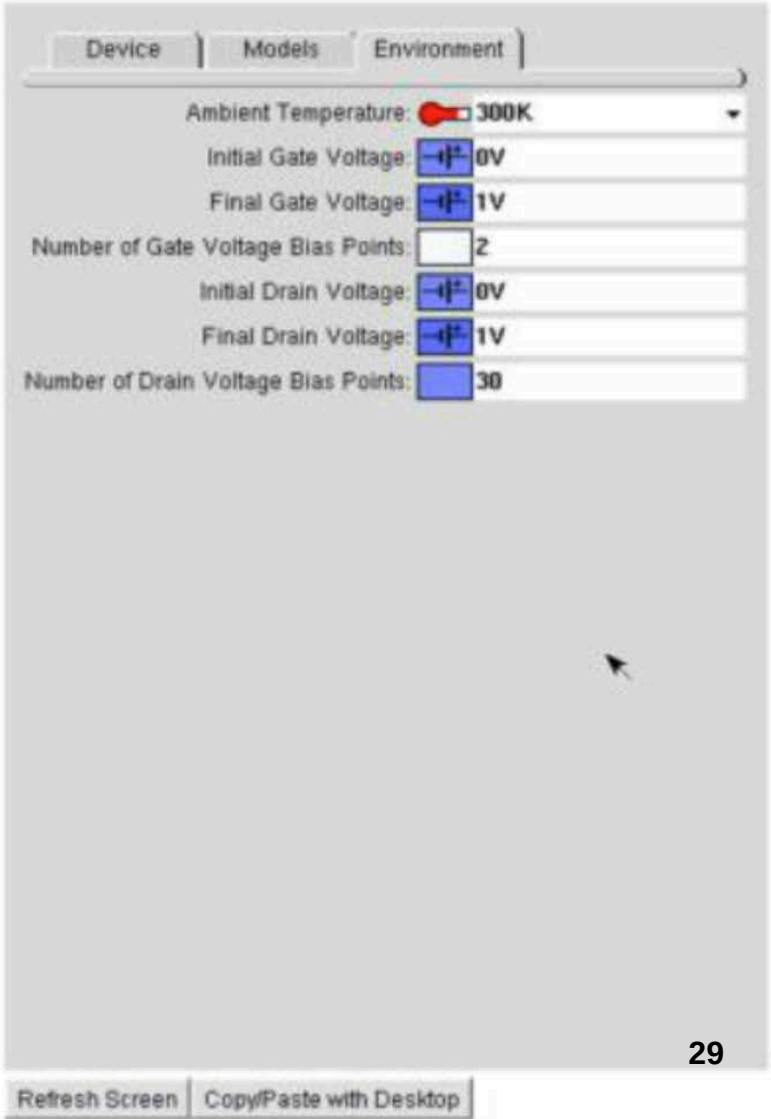
Required Material Parameters:

Material	Effective Electron Mass	Valley Degeneracy
Si	$.19m_0$	2
Ge	$.082m_0$	1
GaAs	$.067m_0$	1
InAs	$.023m_0$	1

4a) Simulated Plot of I_D/I_{ON} vs. V_{DS}

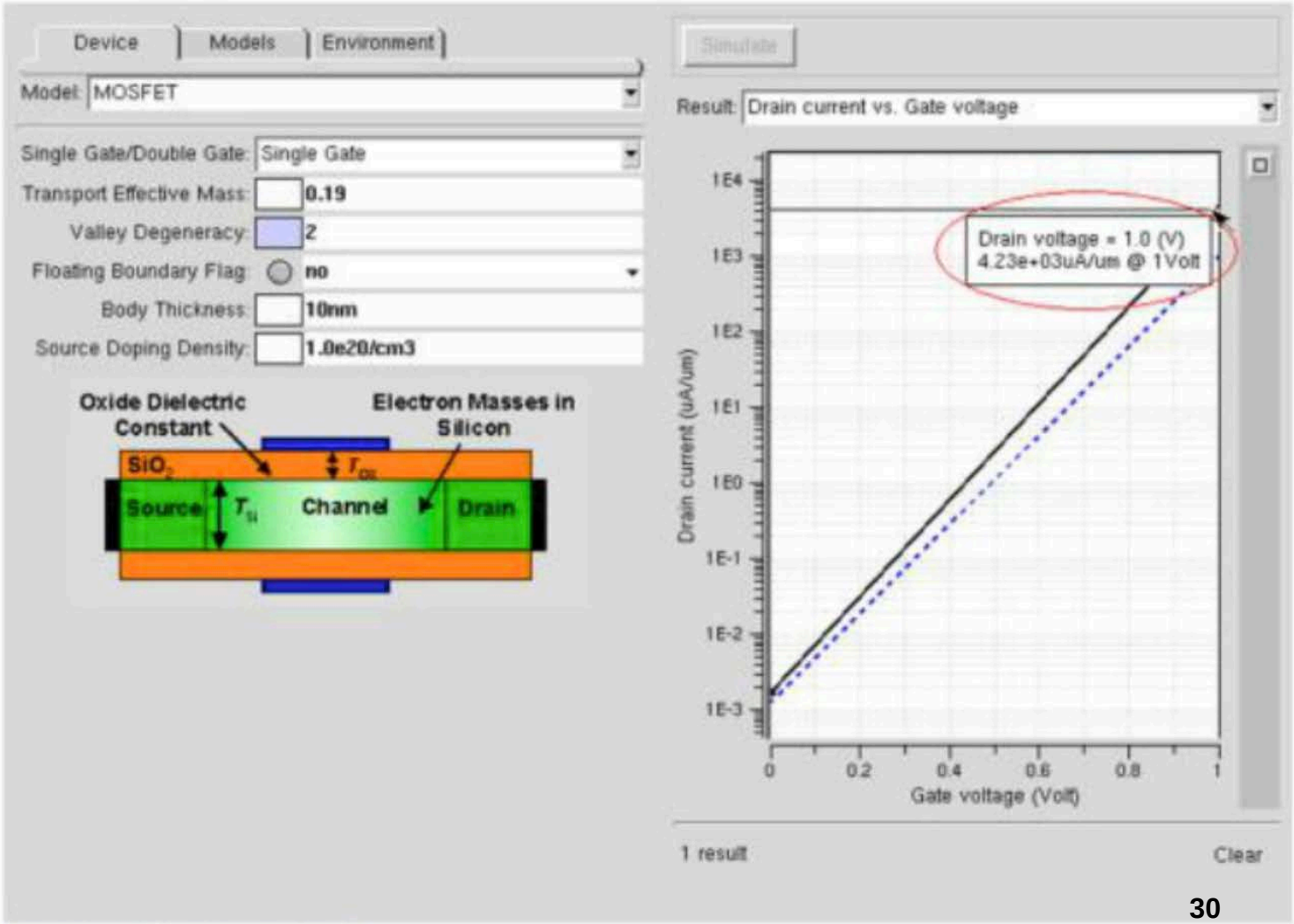
Common Material Parameters and Settings:





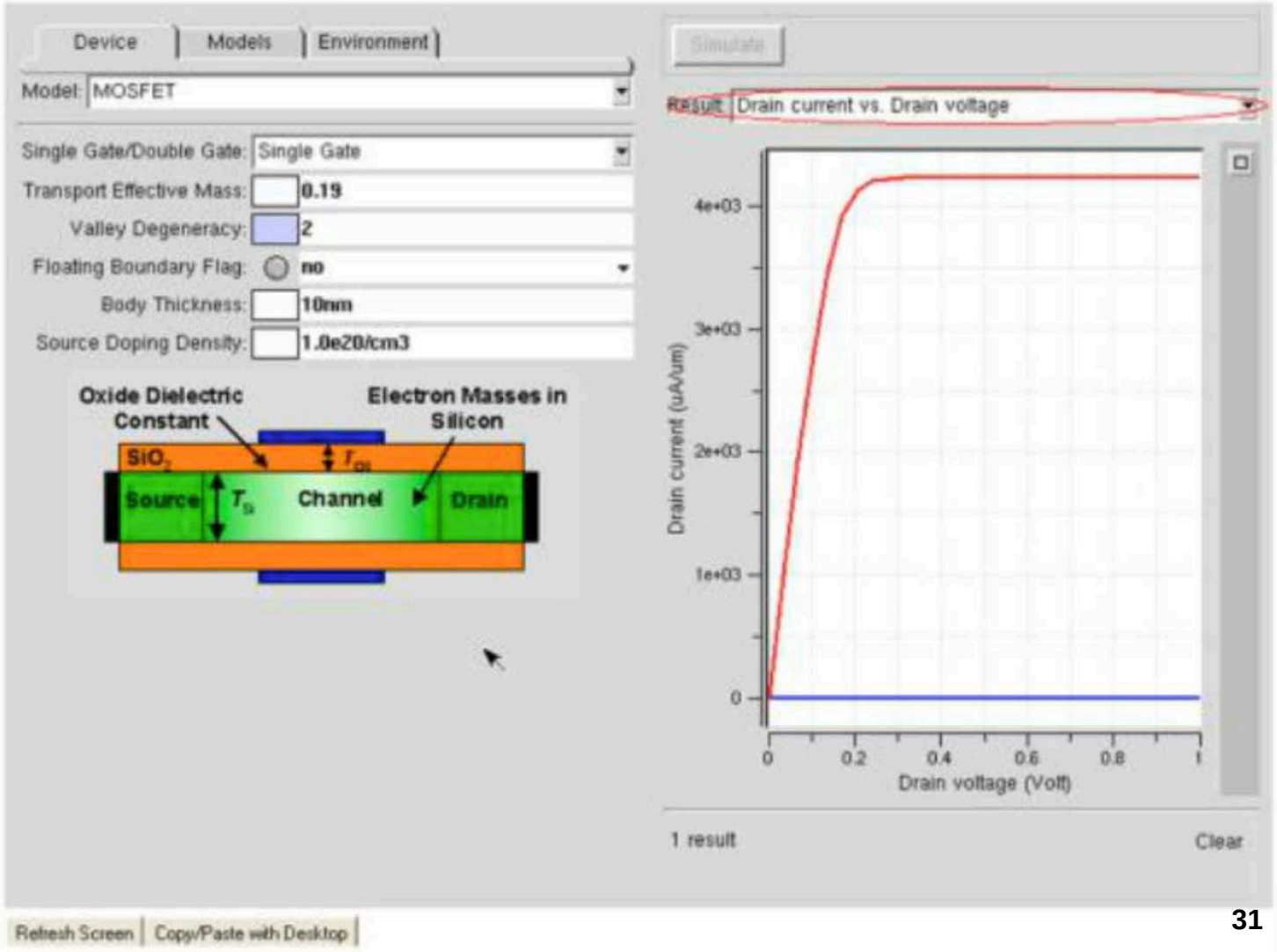
4a) Simulated Plot of I_D/I_{ON} vs. V_{DS}

Material Parameters and Settings for Si,
Result for Si MOSFET: $I_{ON\ Si}$ = 4230A/m



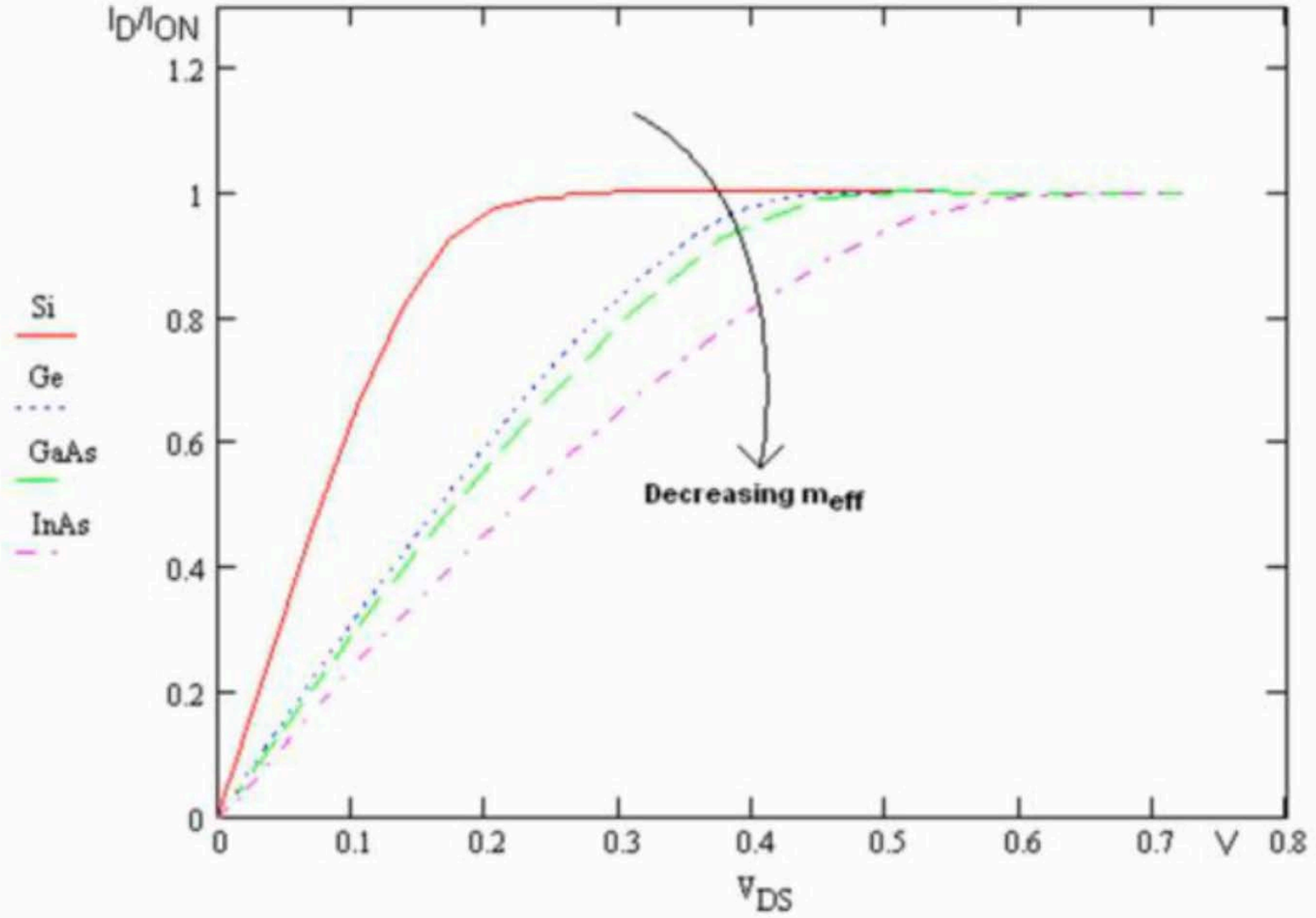
4a) Simulated Plot of I_D/I_{ON} vs. V_{DS}

Obtaining IDS vs. VDS Data Points for Si MOSFET:



4a) Simulated Plot of I_D/I_{ON} vs. V_{DS}

Simulated Plot of I_D/I_{ON} vs. V_{DS} for all MOSFETs:



4b) Explanation for difference in V_{Dsat}

Observation:

m_{eff} decreases ➔ V_{Dsat} increases

Explanation:

1D Electrostatics: $Q = V_G C_G$ C_G is the series capacitance of C_q and C_{ox}

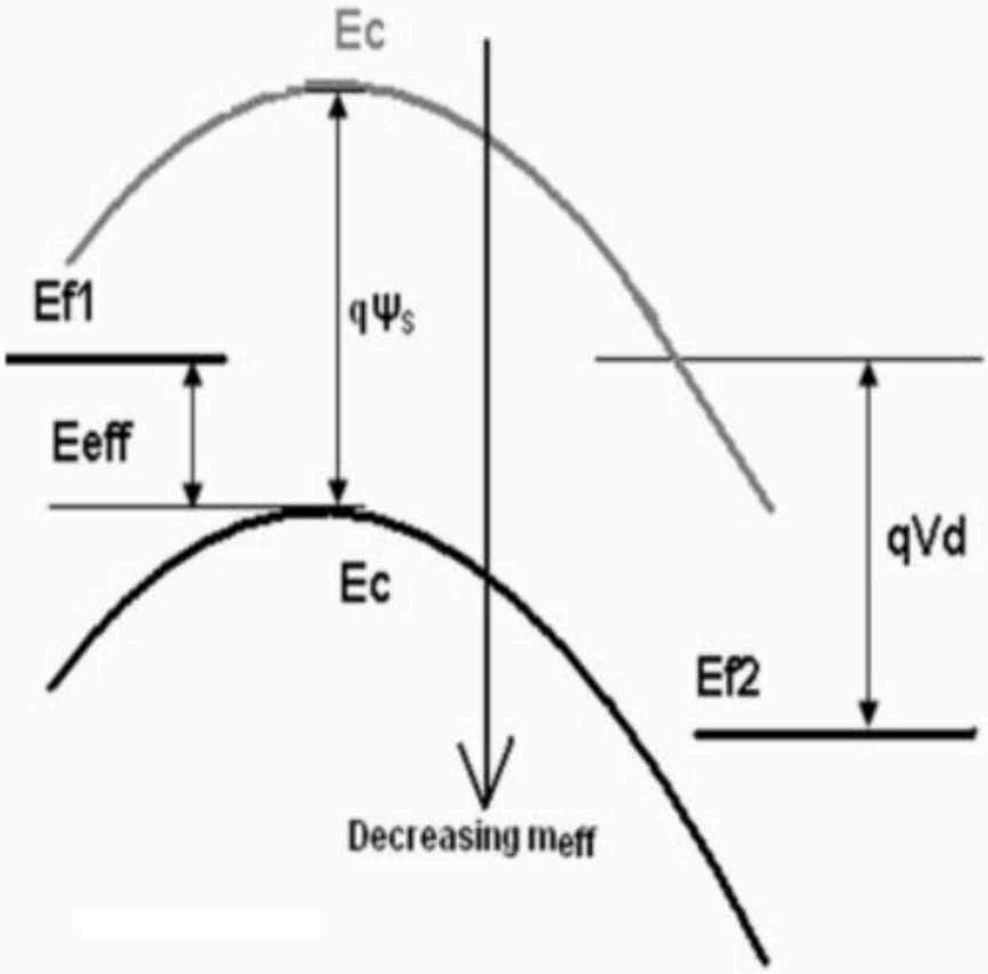
So $\psi_S = C_{ox}/(C_{ox}+C_q)*V_G$

And $C_q = Const^* m_{eff}$,

The smaller C_q is, the larger ψ_S is, the lower the potential barrier height is.

The current saturates when drain voltage exceeds the difference between the source Fermi level and the top of the barrier.

Lower barrier height → higher V_{Dsat}



Problem 5

A silicon n-MOSFET typically delivers about twice the on-current of a silicon p-MOSFET. This difference is commonly attributed to difference in carrier mobility and saturation velocity. What does a ballistic model predict?

5) Simulate a ballistic silicon, n-MOSFET and a ballistic p-MOSFET using 2nm of SiO2 for the gate insulator, *VDD* = 1V, and assuming room temperature operation. For this calculation, you should also use **1D electrostatics** (gate control parameter = 1 and drain control parameter = 0). You will need to identify the appropriate hole effective mass and valley degeneracy.

a) Compare the on-currents of the two MOSFETs and explain the difference. Why does the n-MOSFET give higher current?

b) Compare the low *VDS* channel resistances of the two MOSFETs and explain the difference. Is the ratio of the channel resistances the same as the ratio of the on-currents? Provide a physical explanation for the result.

c) Repeat parts a) and b) for a 0.5nm gate insulator.

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

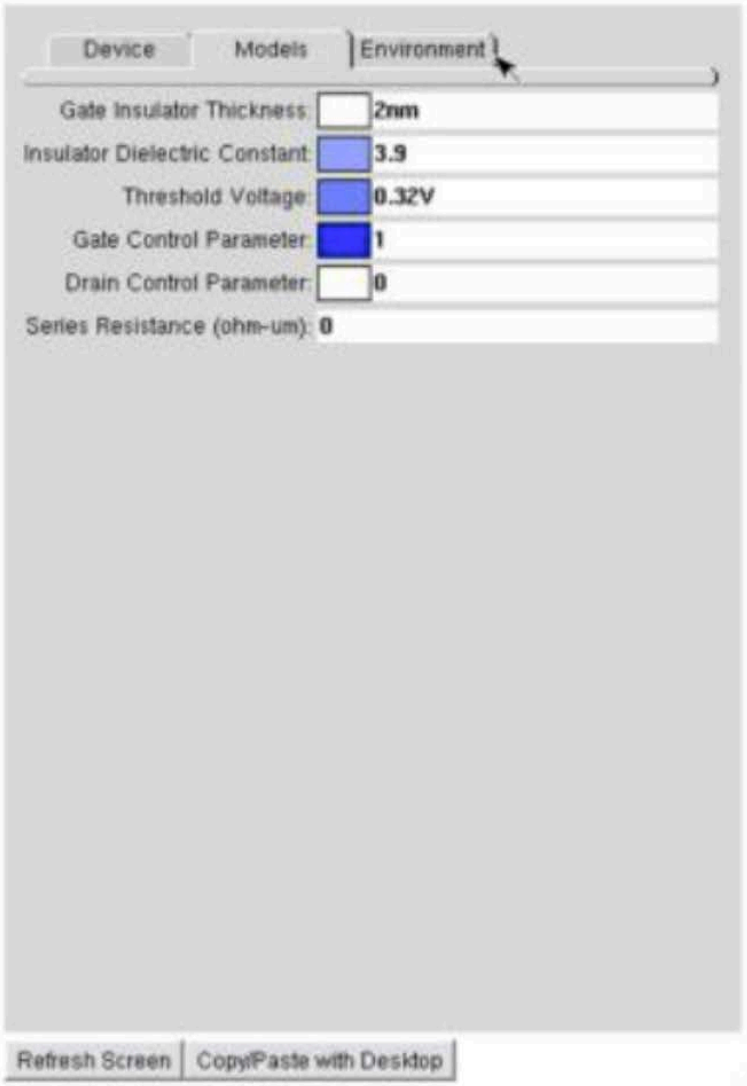
5a) n- vs. p-type on-current comparison, 2nm

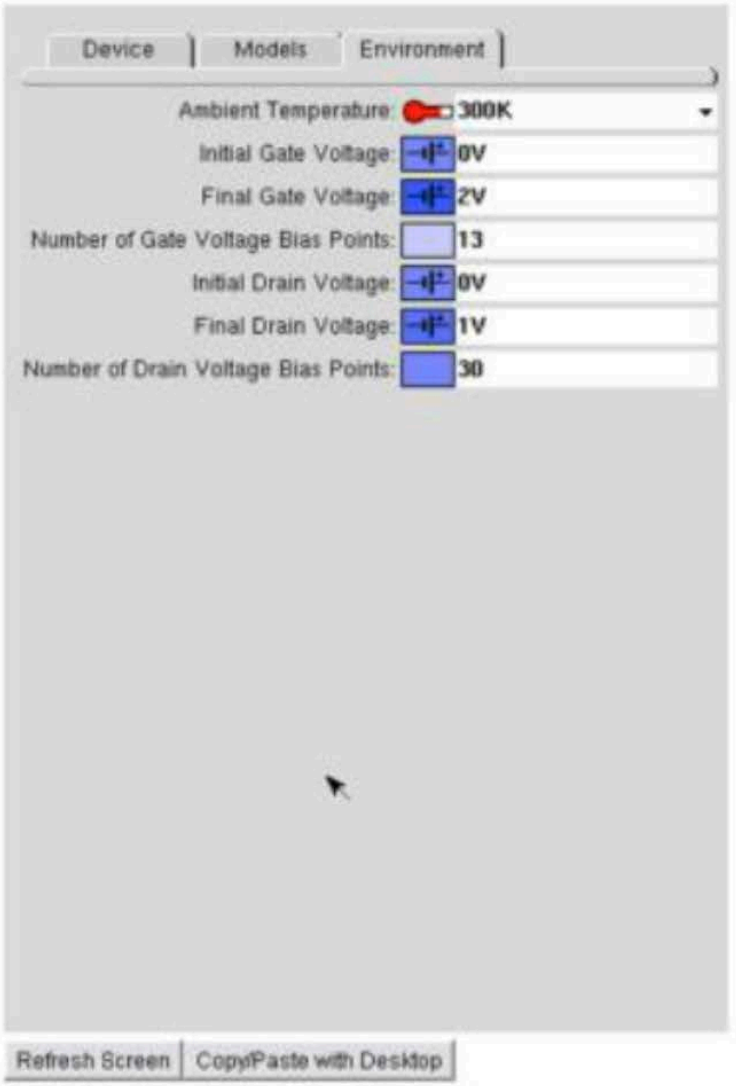
Required Material Parameters:

	Si nMOSFET	Si pMOSFET
Transport Effective Mass	$0.19m_0$	$0.49m_0$
Valley Degeneracy	2	1

5a) n- vs. p-type on-current comparison, 2nm

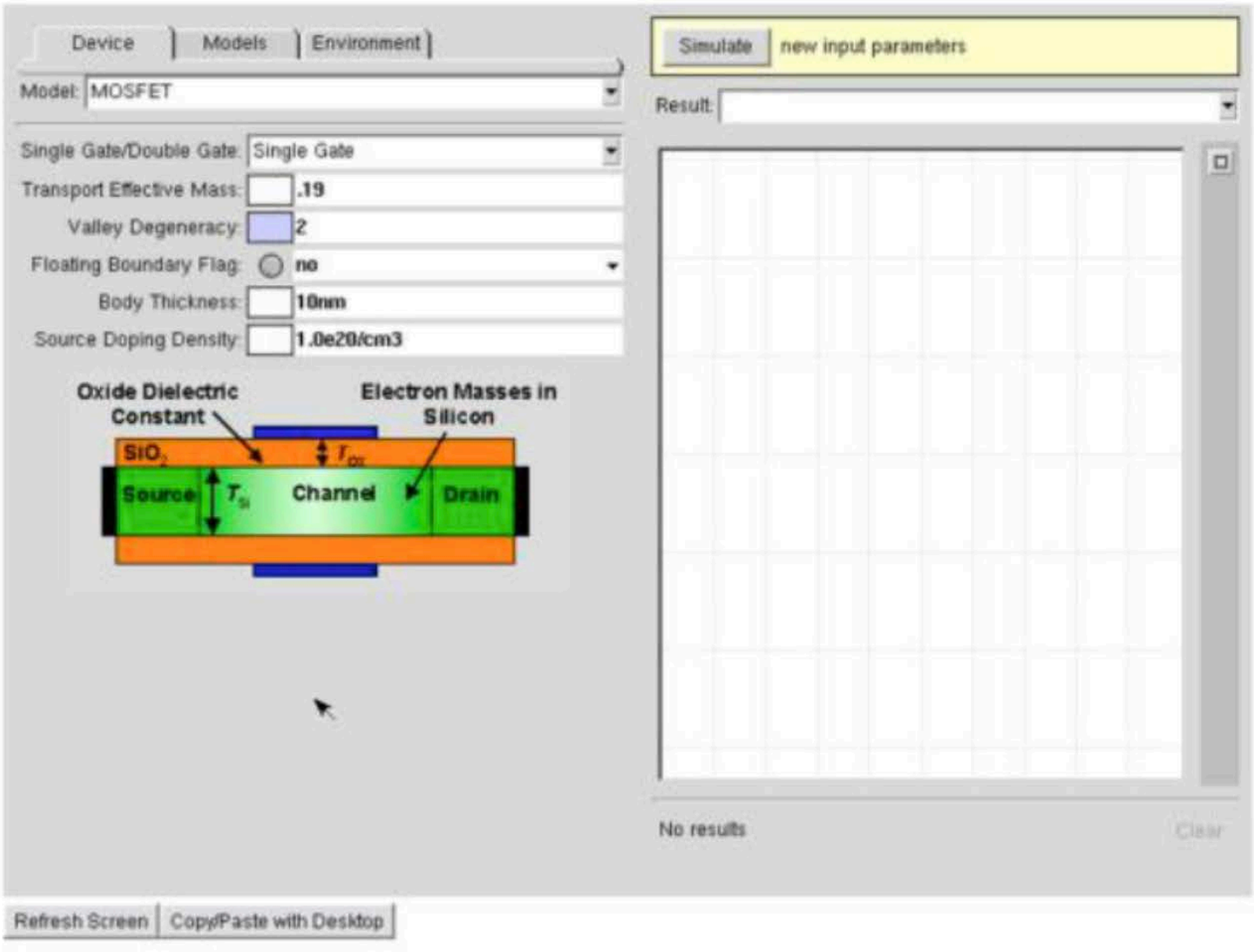
Common Material Parameters and Settings:





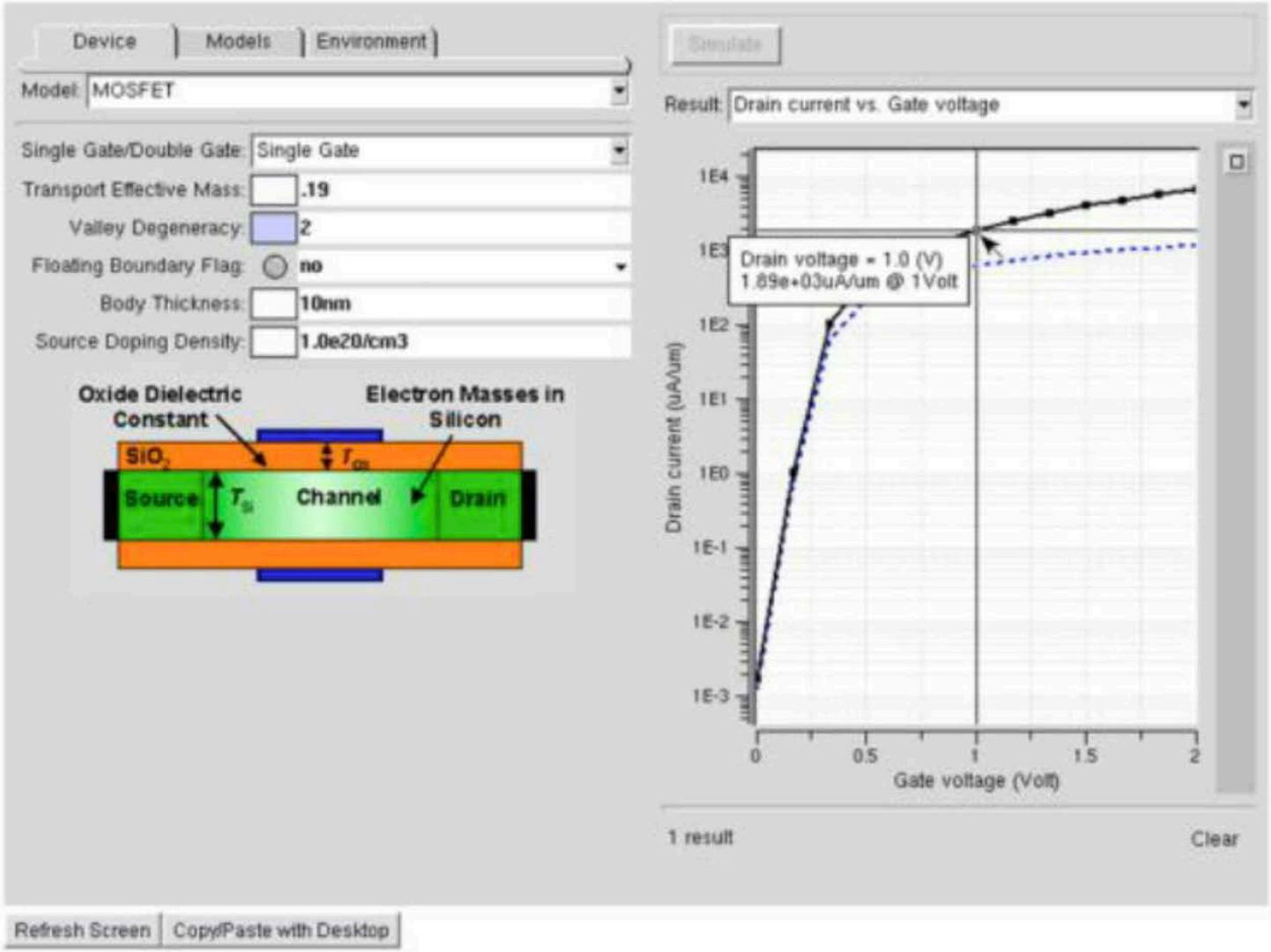
5a) n- vs. p-type on-current comparison, 2nm

Material Parameters and Settings for Si nMOSFET:



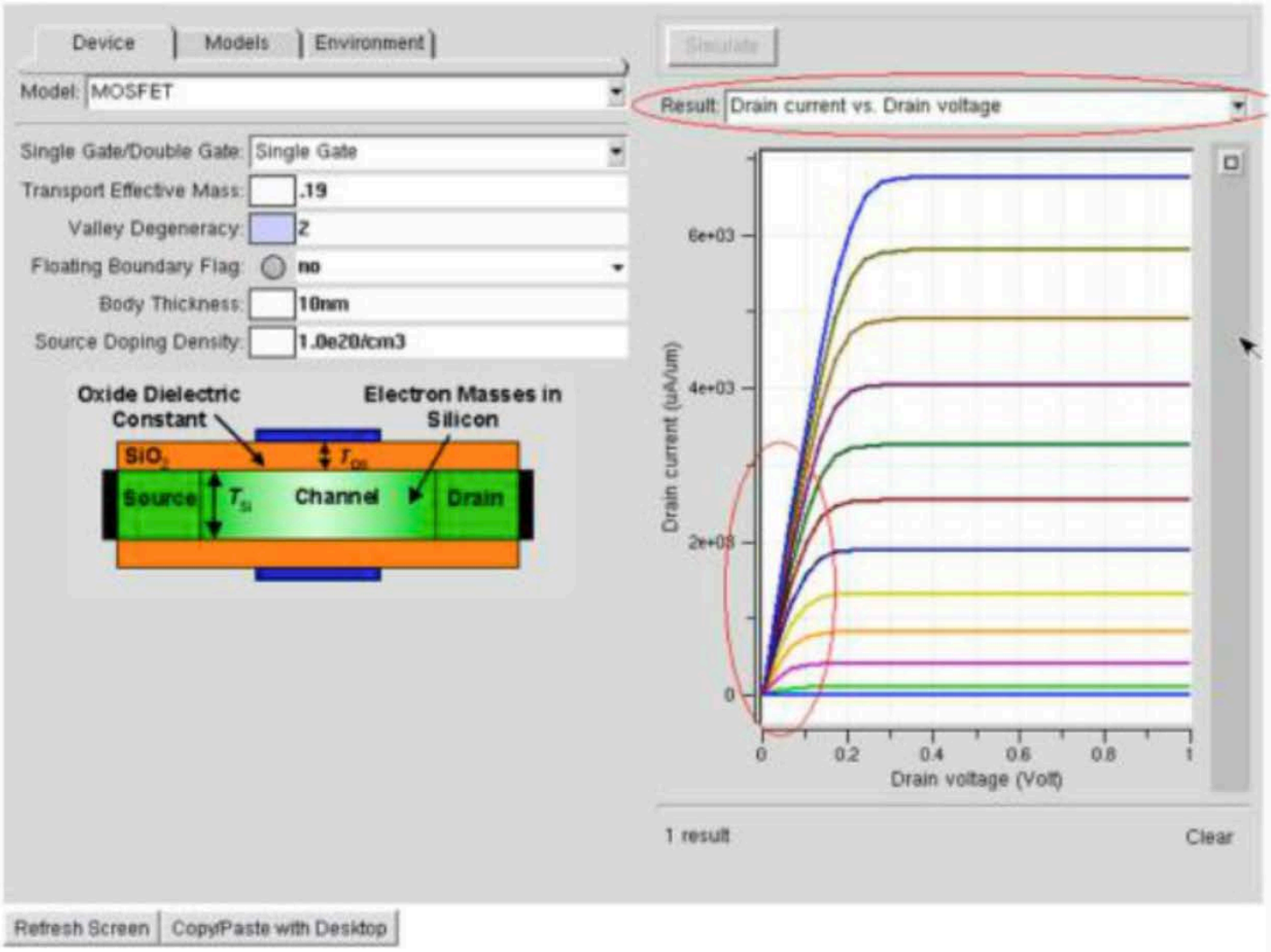
5a) n- vs. p-type on-current comparison, 2nm

Result for Si nMOSFET: I_{ON} = 1.89E3uA/um



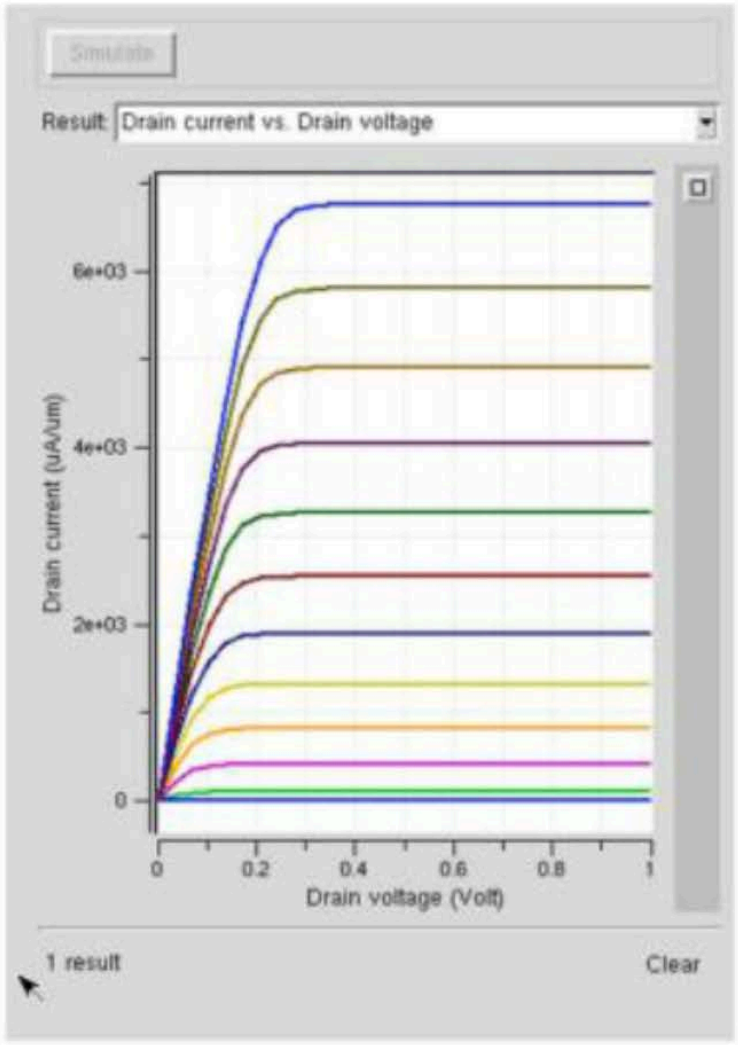
5a) n- vs. p-type on-current comparison, 2nm

Result for Si nMOSFET: $R_{CHANNEL}$ = ?? for V_G = 1V



5a) n- vs. p-type on-current comparison, 2nm

Result for Si nMOSFET: $R_{CHANNEL}$ = 6.26E-5Ωm for V_G = 1V



ID(0.0345V) = 649uA/um
ID(0.069V) = 1.2E3uA/um

$R_{CHANNEL}$ = (0.069V – 0.0345V)/(1.2E3A/m – 649A/m)

$R_{CHANNEL}$ = 6.26E-5Ωm

5a) n- vs. p-type on-current comparison, 2nm

Results for Si nMOSFET and pMOSFET:

	Si nMOSFET	Si pMOSFET
I_{ON}	1.89E3uA/um	1.13E3uA/um
$R_{Channel}$	6.26E-5Ωm	2.1E-4Ωm

5a) n- vs. p-type on-current comparison, 2nm

Comparison for Si nMOSFET and pMOSFET I_{ON}:

	Si nMOSFET	Si pMOSFET
I_{ON}	1.89E3uA/um	1.13E3uA/um
$R_{Channel}$	6.26E-5Ωm	2.1E-4Ωm

$I_{ONn}/I_{ONp} = 1.67$

$I_{ON} \sim 1/\sqrt{m_{eff}}$

$I_{ONn}/I_{ONp} \sim (1/\sqrt{m_{effn}})*(1/\sqrt{m_{effp}})^{-1} = \sqrt{m_{effp}}/\sqrt{m_{effn}}$

$\sqrt{m_{effp}}/\sqrt{m_{effn}} = 1.54$

5b) n- vs. p-type $R_{CHANNEL}$ comparison, 2nm

Comparison for Si nMOSFET and pMOSFET $R_{CHANNEL}$:

	Si nMOSFET	Si pMOSFET
I_{ON}	1.89E3uA/um	1.13E3uA/um
$R_{Channel}$	6.26E-5Ωm	2.1E-4Ωm

$$R_{CHANNELn}/R_{CHANNELp} = .298$$

5c) n- vs. p-type comparisons, .5nm

Comparison for Si nMOSFET and pMOSFET at 0.5nm:

	Si nMOSFET	Si pMOSFET
I_{ON}	8.73E3uA/um	5.46E3uA/um
$R_{Channel}$	2.56E-5Ωm	3.56E-4Ωm

$I_{ONn}/I_{ONp} = 1.6$

$I_{ONn}/I_{ONp} = n_{vn}m_{effn}^{*}\sqrt{m_{effp}}/(n_{vp}m_{effp}^{*}\sqrt{m_{effn}})$ if $C_G \rightarrow C_Q$

$I_{ONn}/I_{ONp} = 1.2$ if $C_G \rightarrow C_Q$

$R_{CHANNELn}/R_{CHANNELp} = .719$

Problem 6

In FETToy, two-dimensional electrostatics is treated with a simple circuit model and two parameters, a gate control parameter and a drain control parameter.

6) Simulate a ballistic silicon, n-MOSFET using an insulator thickness of 2 nm (SiO2) and *VDD* = 1V, and assuming room temperature operation.

6a) Set the gate control parameter to 1.0 and the drain control parameter to 0.0 and run a simulation. Then examine the plot of charge, Q, vs. *VGS* at high and low *VDS*. Explain what determines the slope of the two plots and how you can calculate the slope by hand. Also examine the charge vs. *VDS* plot and explain why it is not constant.

6b) Adjust the gate and drain control parameters to give a subthreshold swing of *S* = 100 mV/decade and a DIBL of 100 mV/V. Repeat the simulation, compare the results to part a) and explain the differences.

6c) Repeat parts a) and b) but this time use an insulator thickness of 0.5 nm.

Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Material Parameters and Settings:

Device | Models | Environment

Model: MOSFET

Single Gate/Double Gate: Single Gate

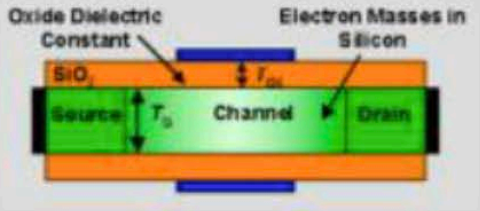
Transport Effective Mass: 0.19

Valley Degeneracy: 2

Floating Boundary Flag: no

Body Thickness: 10nm

Source Doping Density: 1.0e20/cm3



Device | Models | Environment

Gate Insulator Thickness: 2nm

Insulator Dielectric Constant: 3.9

Threshold Voltage: 0.32V

Gate Control Parameter: 1

Drain Control Parameter: 0

Series Resistance (ohm-um): 0

Device | Models | Environment

Ambient Temperature: 300K

Initial Gate Voltage: 0V

Final Gate Voltage: 2.0V

Number of Gate Voltage Bias Points: 30

Initial Drain Voltage: 0V

Final Drain Voltage: 2V

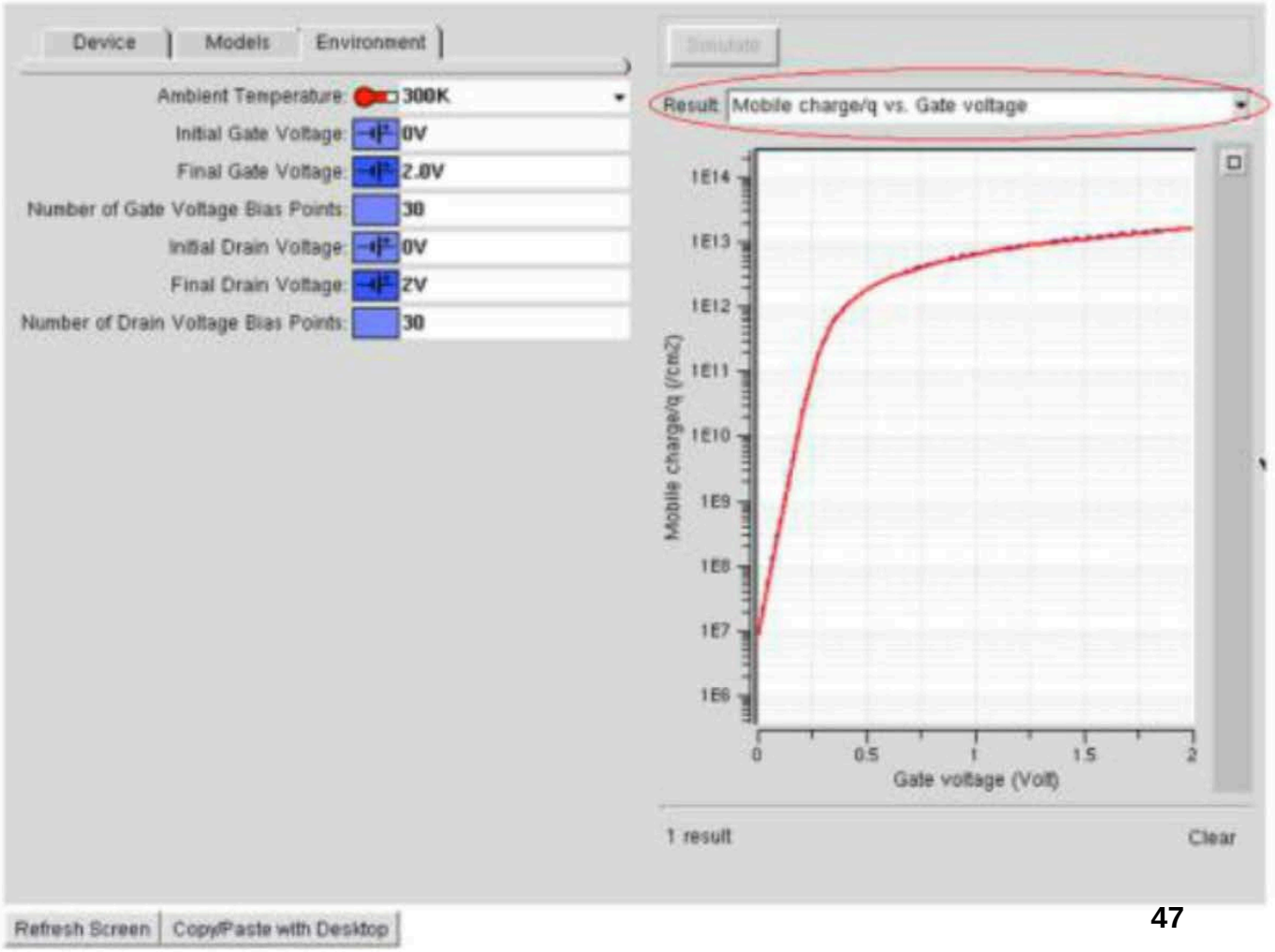
Number of Drain Voltage Bias Points: 30

6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:

Slope for V_{DS} = 2V: $slope_h$ = ??

Slope for V_{DS} = 0.069V: $slope_l$ = ??

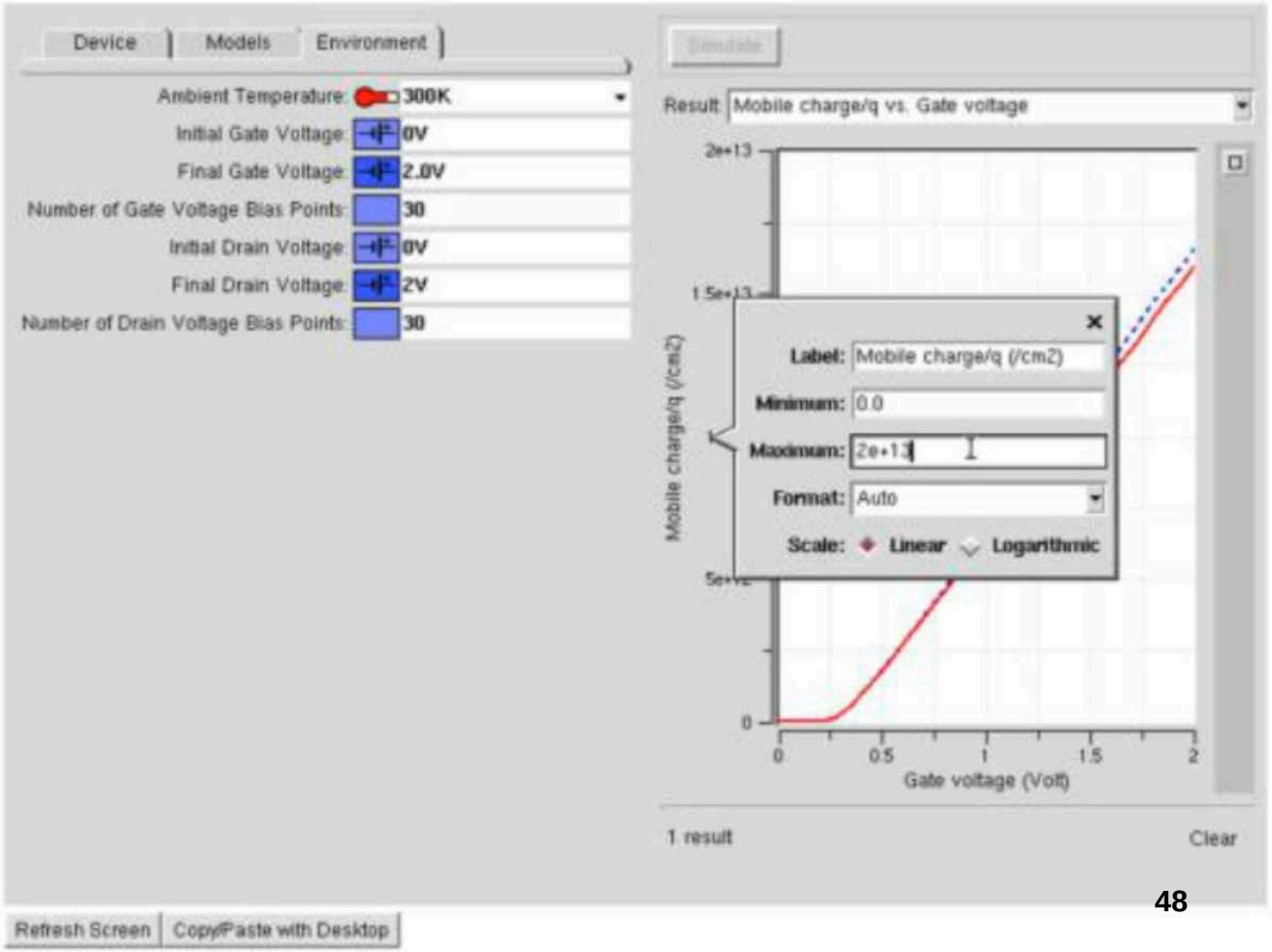


6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:

Slope for V_{DS} = 2V: **$slope_h$ = ??**

Slope for V_{DS} = 0.069V: **$slope_l$ = ??**

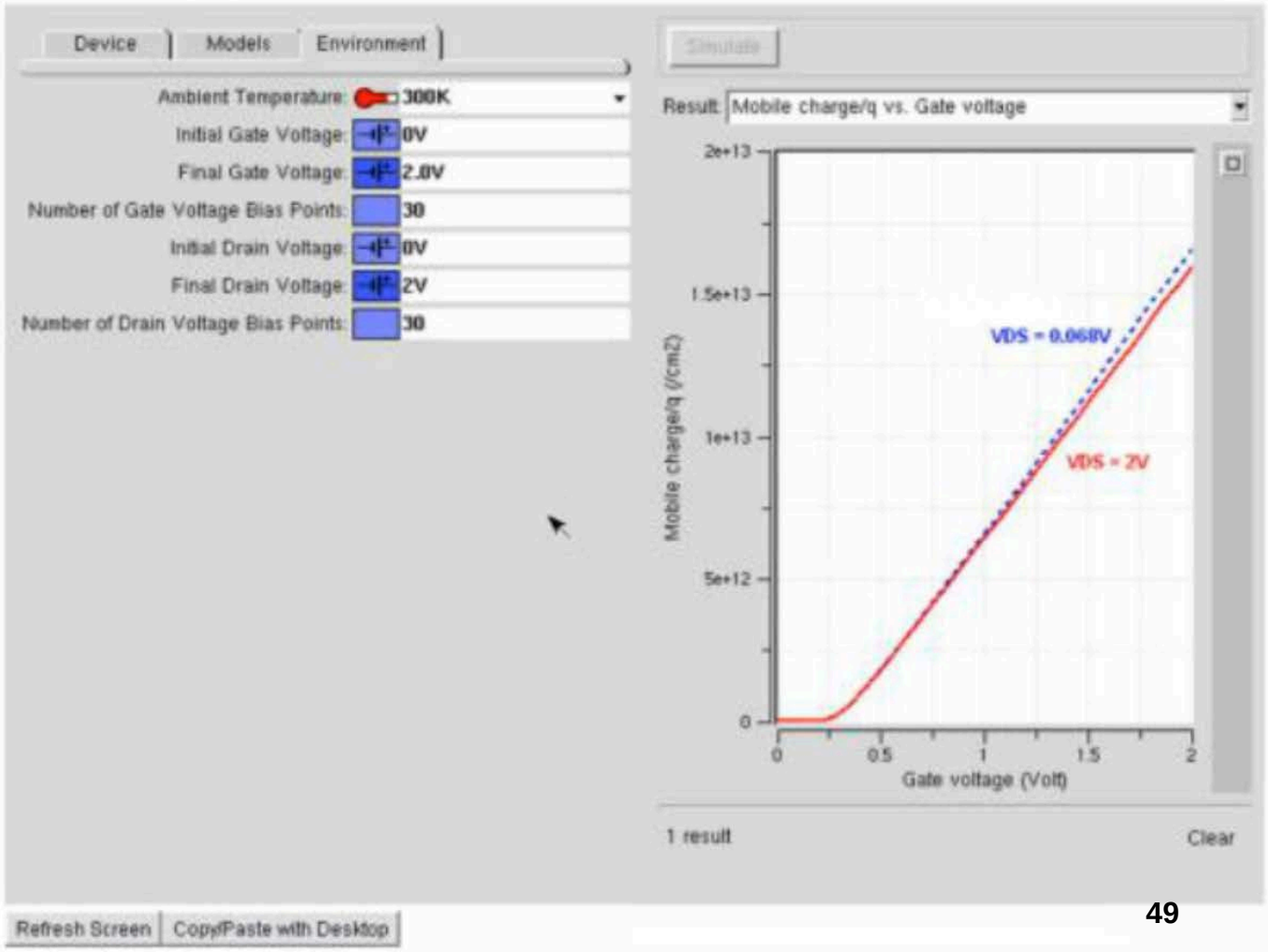


6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:

Slope for V_{DS} = 2V: $slope_h$ = 1.54E-6 F/cm²

Slope for V_{DS} = 0.069V: $slope_l$ = 1.58E-6F/cm²



6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Determining the Slope of Charge vs. Gate Voltage by Hand:

1D Electrostatics ➔ $C_D = C_S = 0$

Since $V_G = Q/C_G$

$Q = C_G * V_G$

Slope is determined by C_G, **$C_G \rightarrow C_{OX}$ if $C_Q >> C_{OX}$**

$C_{OX} = 3.9\varepsilon_0/T_{OX} = 1.73E\text{-}6F/cm^2$

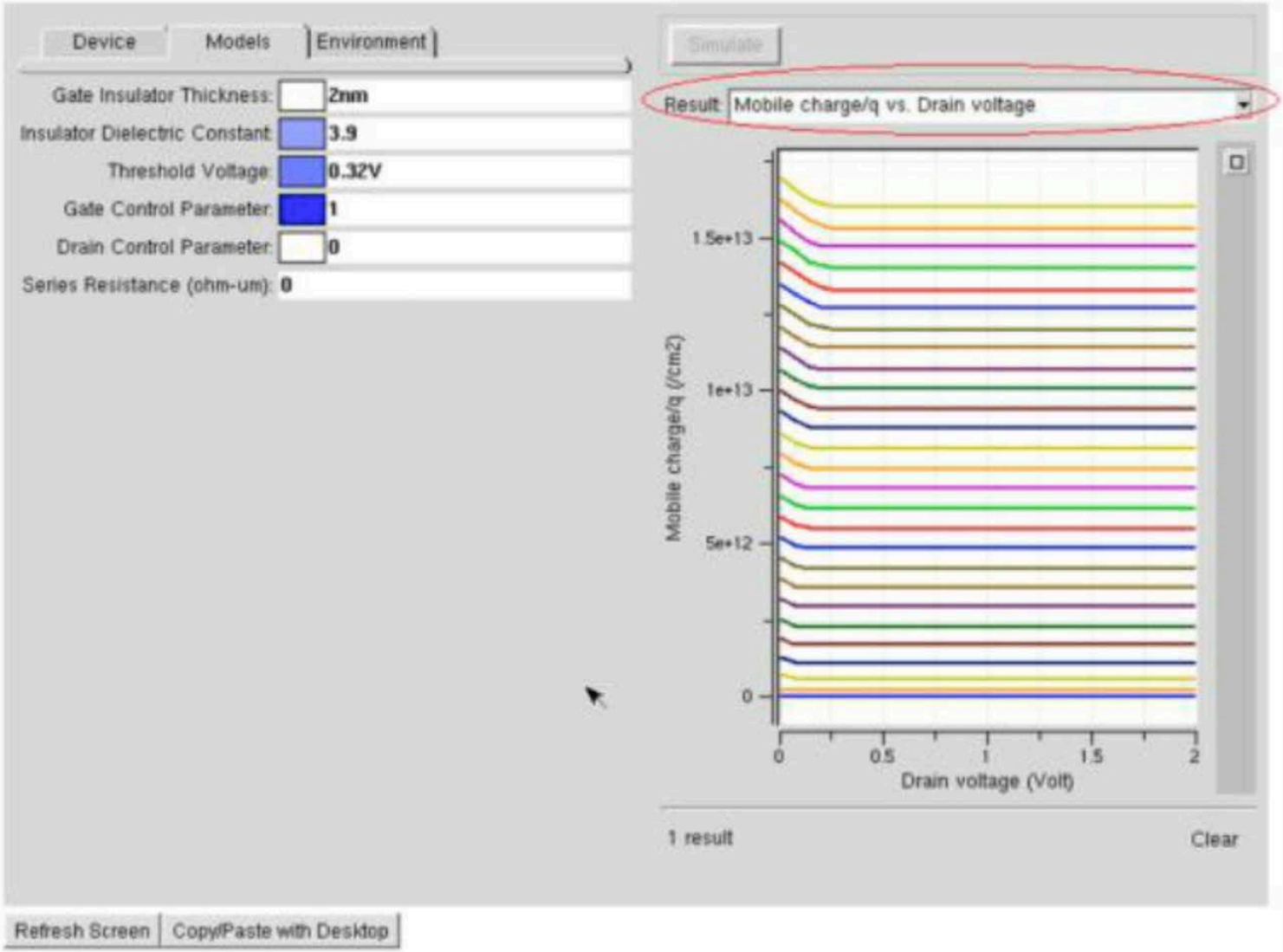
$slope_h = 1.54E\text{-}6F/cm^2$ **$slope_l = 1.58E\text{-}6F/cm^2$**

$C_Q = 2*q^{2}*m_{eff}/(\pi*h_{bar}^{2}) = 2.54E\text{-}5F/cm^2$

$C_G = C_{OX}C_Q/(C_{OX}+C_Q) = 1.45E\text{-}6F/cm^2$

6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:



6a) 1D Electrostatics: Charge vs. Voltage, 2nm

Explanation for Q not constant as V_{DS} increases for 1D electrostatic case:

$N = N_{2D}WL/2[F_0(\eta_{F1}) + F_0(\eta_{F2})]$

$\psi_S = C_{OX}/C_{\Sigma}{}^*V_G - q(N-N_0)/C_{\Sigma}$ — independent of V_D

$\eta_{F1} = (E_{F1} - E_C{}^{FB} + q\psi_S)/(k_bT)$ — independent of V_D

$\eta_{F2} = \eta_{F1} - qV_D/(k_bT)$ — dependent on V_D

$F_j(\eta) \rightarrow e^{\eta}$ as $\eta \rightarrow -\infty$

$F_0(\eta_{F2}) \rightarrow 0$ as $\eta_{F2} \rightarrow -\infty$

$\eta_{F2} \rightarrow -\infty$ as $V_D \rightarrow \infty$

$N = N_{2D}WL/2[F_0(\eta_{F1})]$ for V_D large — independent of V_D

6b) 2D Electrostatics: Charge vs. Voltage, 2nm

Gate Control Parameter:

$S = 100\text{mV/decade}$

$\alpha_G = (2.3k_BT/q)/S$

$\underline{\alpha_G = 0.595}$

Drain Control Parameter:

$DIBL = 100\text{mV/V}$

$\alpha_D = (2.3k_BT*DIBL)/(q*S)$

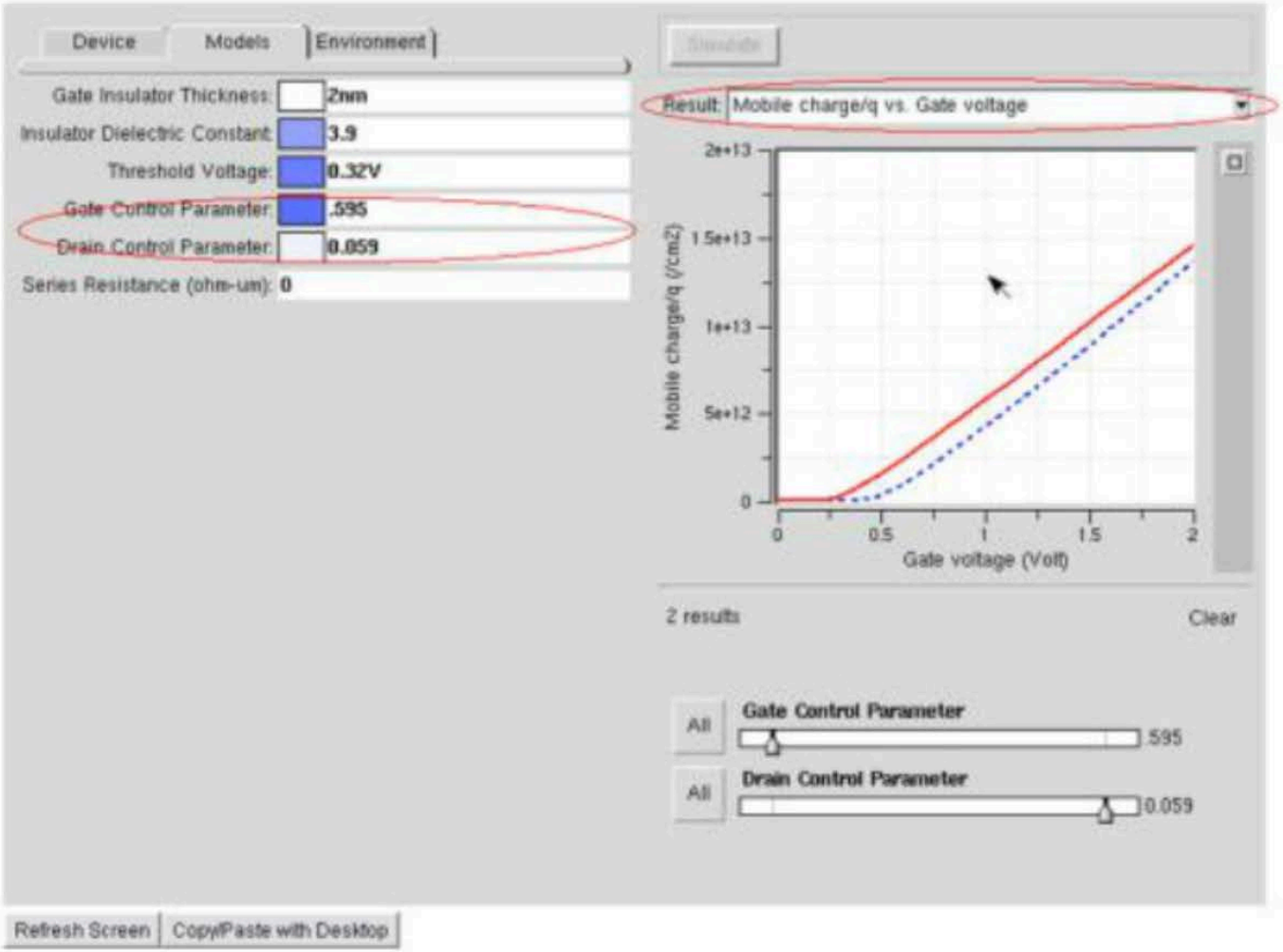
$\underline{\alpha_D = 0.059}$

6b) 2D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:

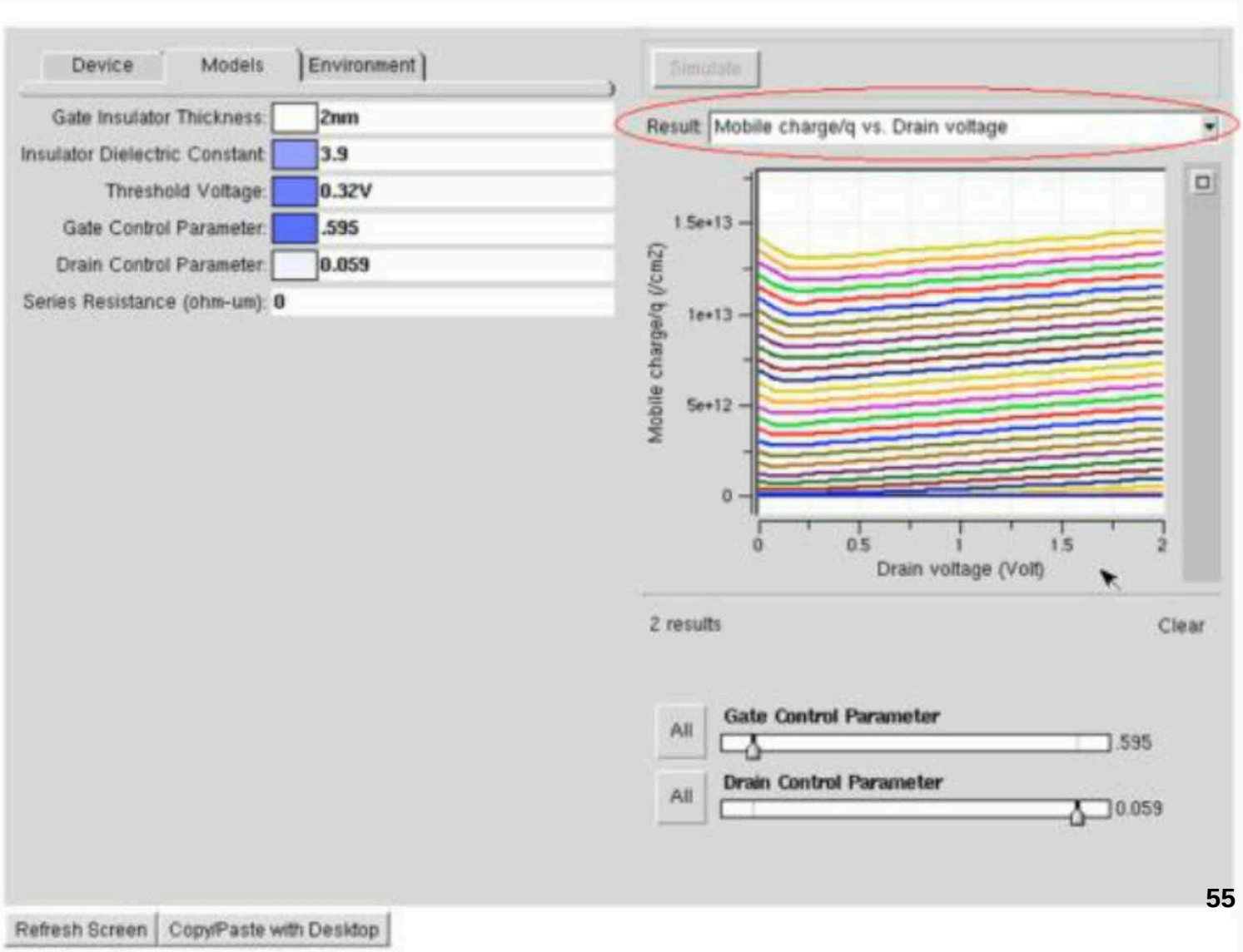
Slope for V_{DS} = 2V: $slope_h$ = 1.40E-6F/cm^2 C_{OX} = 1.73E-6F/cm^2

Slope for V_{DS} = 0.069V: $slope_l$ = 1.49E-6F/cm^2



6b) 2D Electrostatics: Charge vs. Voltage, 2nm

Simulation Result:



6c) 1D/2D Electrostatics: Charge vs. Voltage, 0.5nm

Material Parameters and Settings:

Device | Models | Environment

Model: MOSFET

Single Gate/Double Gate: Single Gate

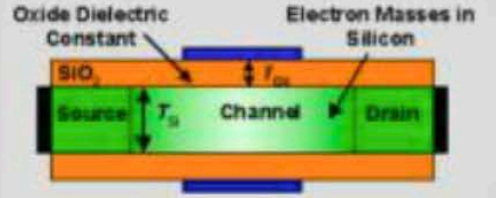
Transport Effective Mass: 0.19

Valley Degeneracy: 2

Floating Boundary Flag: no

Body Thickness: 10nm

Source Doping Density: 1.0e20/cm3



Device | Models | Environment

Gate Insulator Thickness: 6.5nm

Insulator Dielectric Constant: 3.9

Threshold Voltage: 0.32V

Gate Control Parameter: 1

Drain Control Parameter: 0

Series Resistance (ohm-um): 0

Device | Models | Environment

Ambient Temperature: 300K

Initial Gate Voltage: 0V

Final Gate Voltage: 2.0V

Number of Gate Voltage Bias Points: 30

Initial Drain Voltage: 0V

Final Drain Voltage: 2V

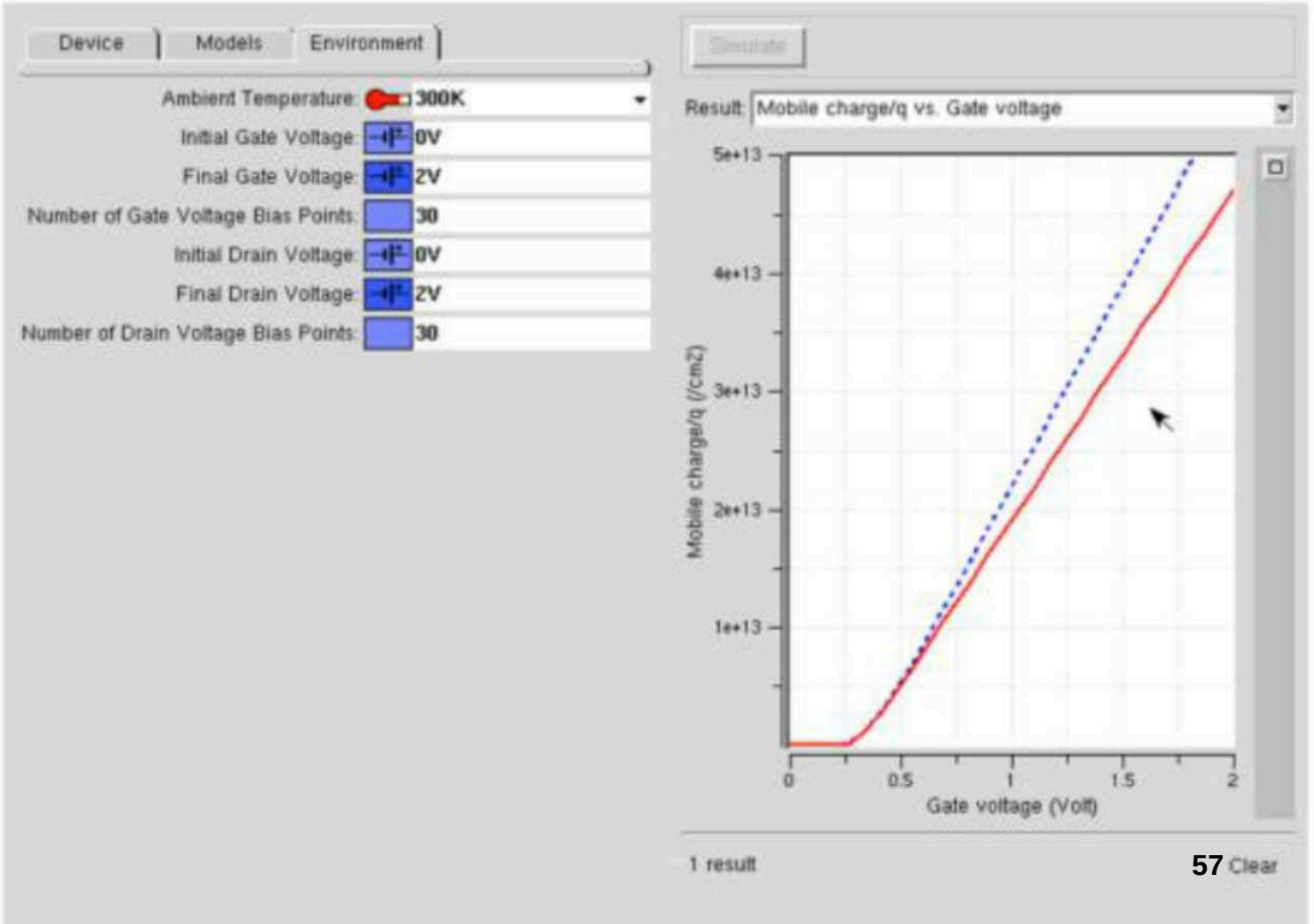
Number of Drain Voltage Bias Points: 30

6c) 1D/2D Electrostatics: Charge vs. Voltage, .5nm

Simulation Result, 1D Electrostatics:

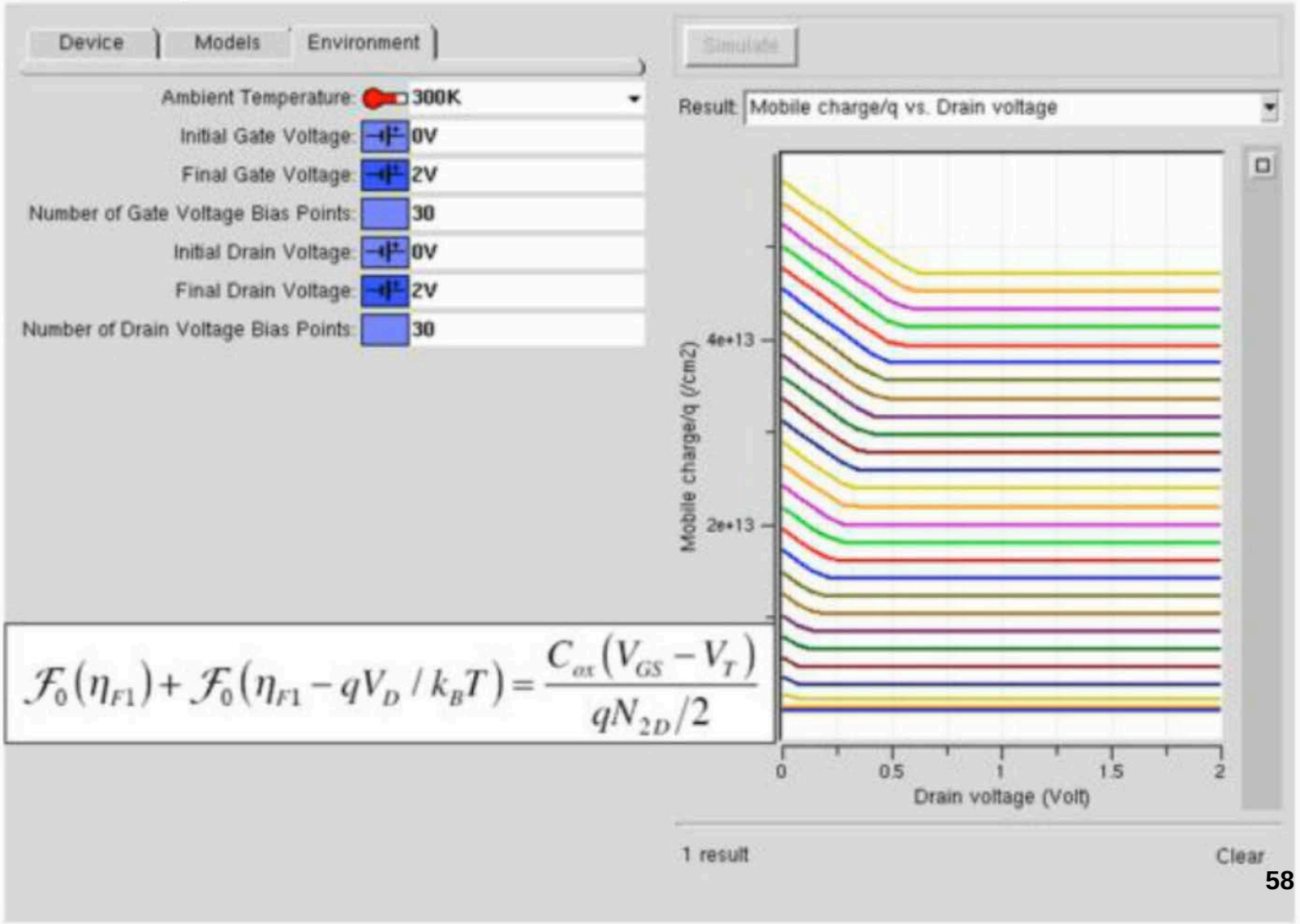
Slope for V_{DS} = 2V: $slope_h$ = 4.50E-6F/cm² C_{OX} = 6.91E-6F/cm²

Slope for V_{DS} = 0.069V: $slope_l$ = 5.46E-6F/cm² C_G = 5.43E-6F/cm²



6c) 1D/2D Electrostatics: Charge vs. Voltage, .5nm

Simulation Result, 1D Electrostatics:



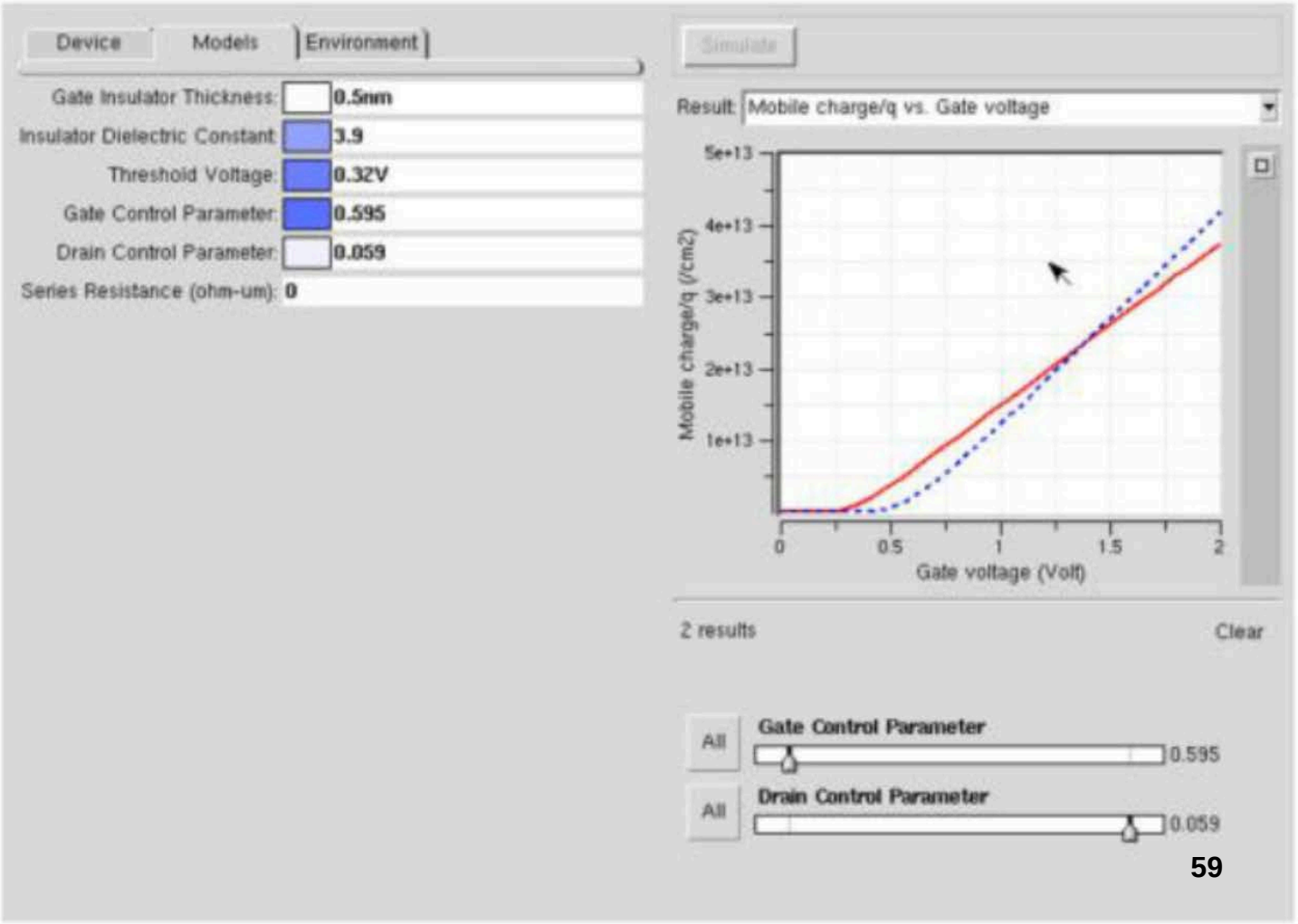
$$\mathcal{F}_0(\eta_{F1}) + \mathcal{F}_0(\eta_{F1} - qV_D / k_B T) = \frac{C_{ox}(V_{GS} - V_T)}{qN_{2D}/2}$$

6c) 1D/2D Electrostatics: Charge vs. Voltage, .5nm

Simulation Result, 2D Electrostatics:

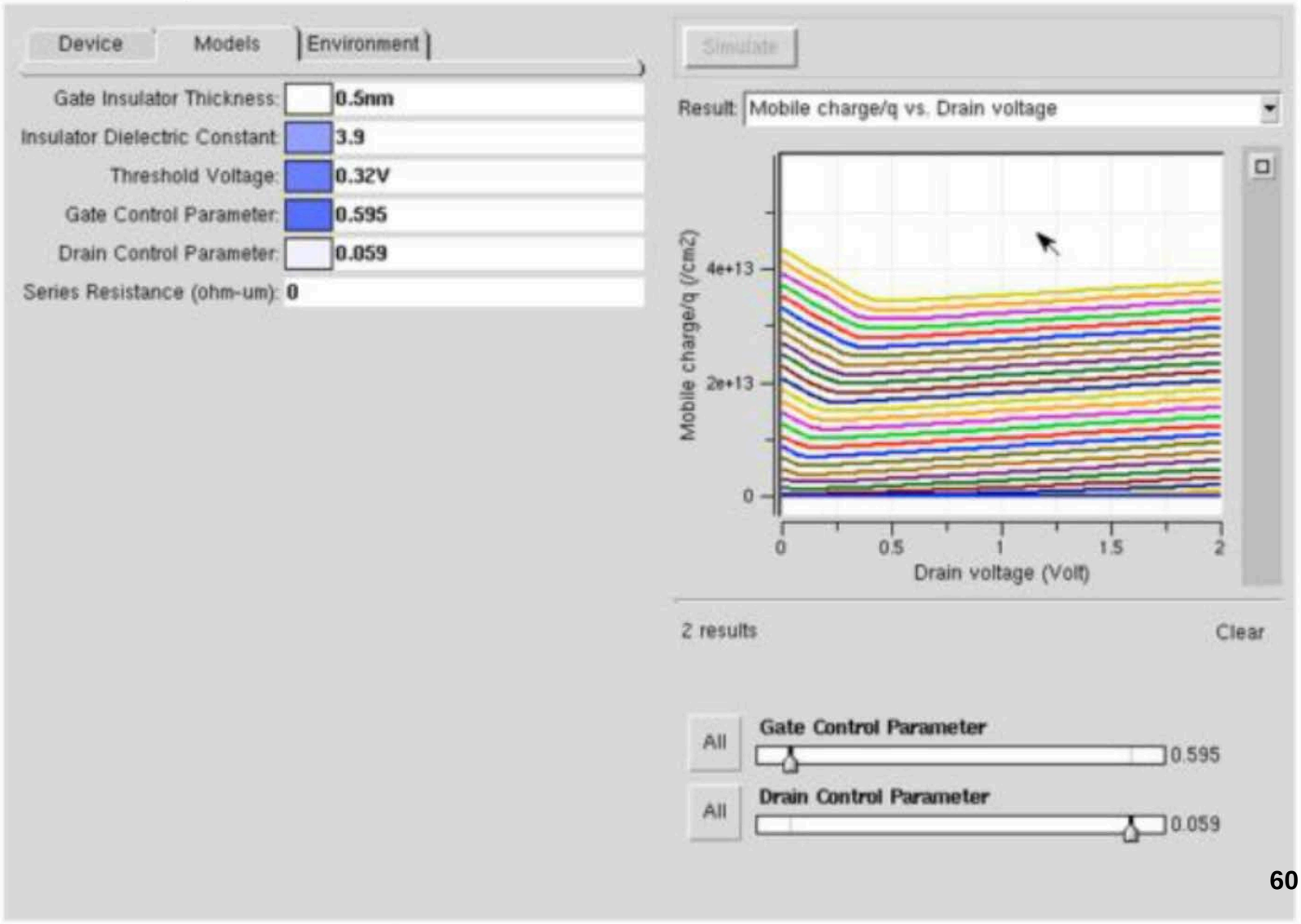
Slope for V_{DS} = 2V: $slope_h$ = 3.62E-6F/cm^2 C_{OX} = 6.91E-6F/cm^2

Slope for V_{DS} = 0.069V: $slope_l$ = 4.70E-6F/cm^2 C_G = 5.43E-6F/cm^2



6c) 1D/2D Electrostatics: Charge vs. Voltage, .5nm

Simulation Result, 2D Electrostatics:



Problem 7

Nanowire transistors are getting a lot of attention these days. They seem to operate more Nearly as SB FETs than as MOSFETs, but it's interesting so see what might happen if Nanowire MOSFETs can be realized. The exercise below will get you calibrated on silicon Nanowire MOSFETs.

7) Examine the *I-V* characteristics of a hypothetical silicon nanowire MOSFET. Assume D = 1nm and that the insulator is 2 nm of SiO2 and that *VDD* = 0.5V. Use an approximate threshold voltage of *VT* = 0.2V and assume room temperature operation.

a) Compute *ID* vs. *VDS* at *T* = 300K and compare the low-*VDS* drain conductance, GD with the quantum conductance, $4e^2/h$.

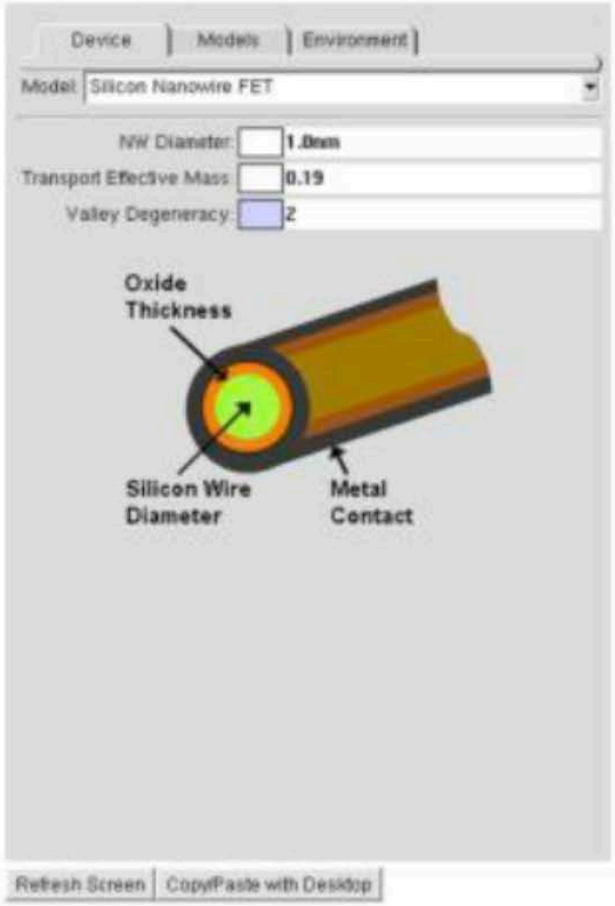
b) Repeat problem i) but at *T* = 77K. The channel conductance vs. *VGS* is strikingly different than a conventional MOSFET. Explain how.

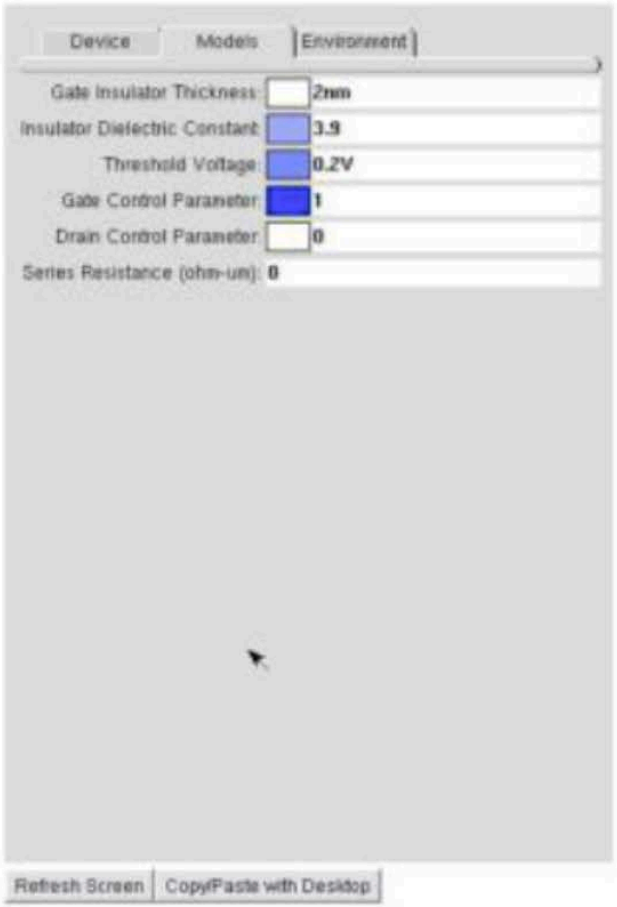
c) The on-current can be written as ID = CG<v(0)>(VGS – VT). Deduce CG, <v(0)>, and VT.

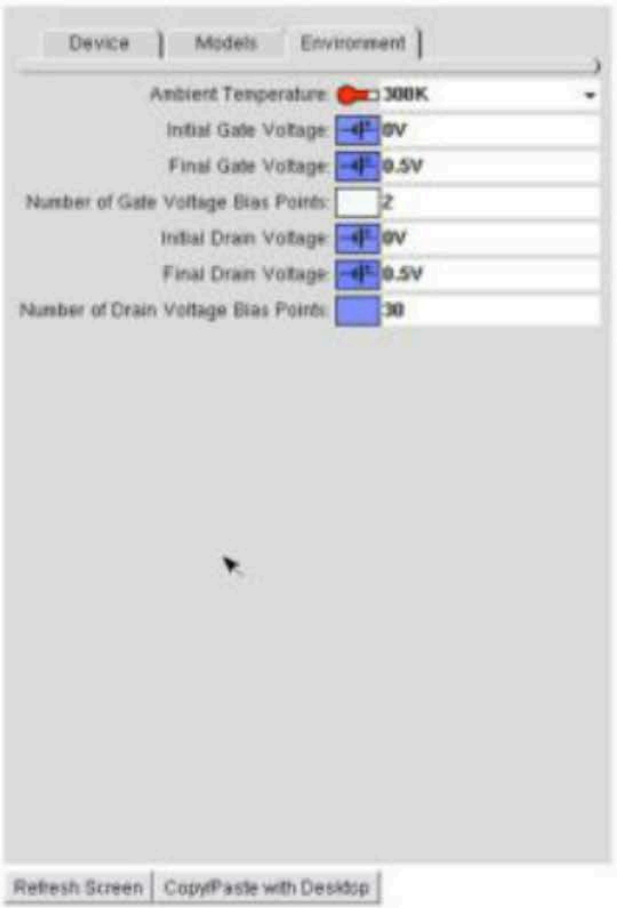
Acknowledgement: The problem is provided by Prof. Mark Lundstrom, Purdue University

7a) Silicon Nanowire FET at 300K

Material Parameters and Settings:

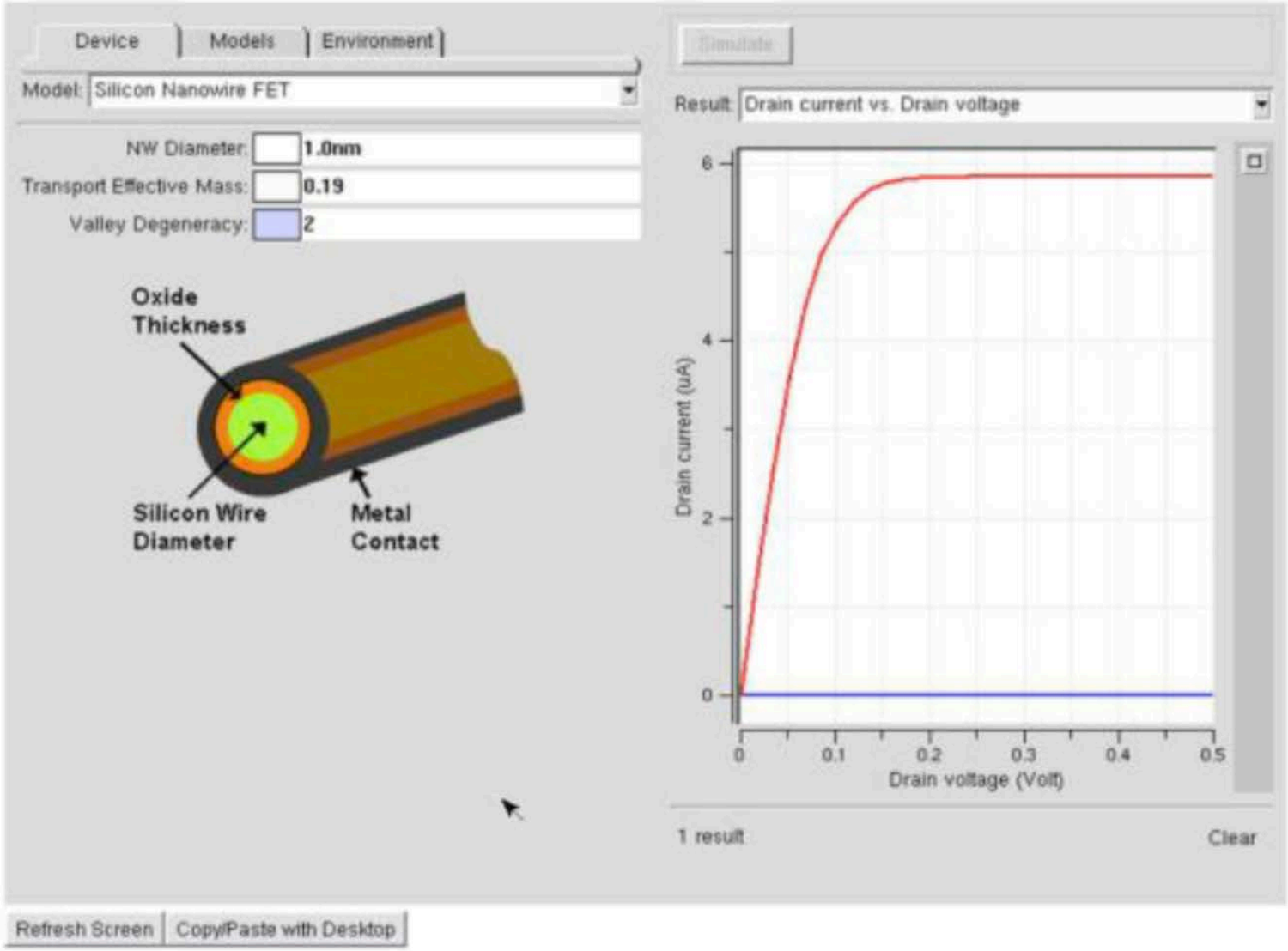






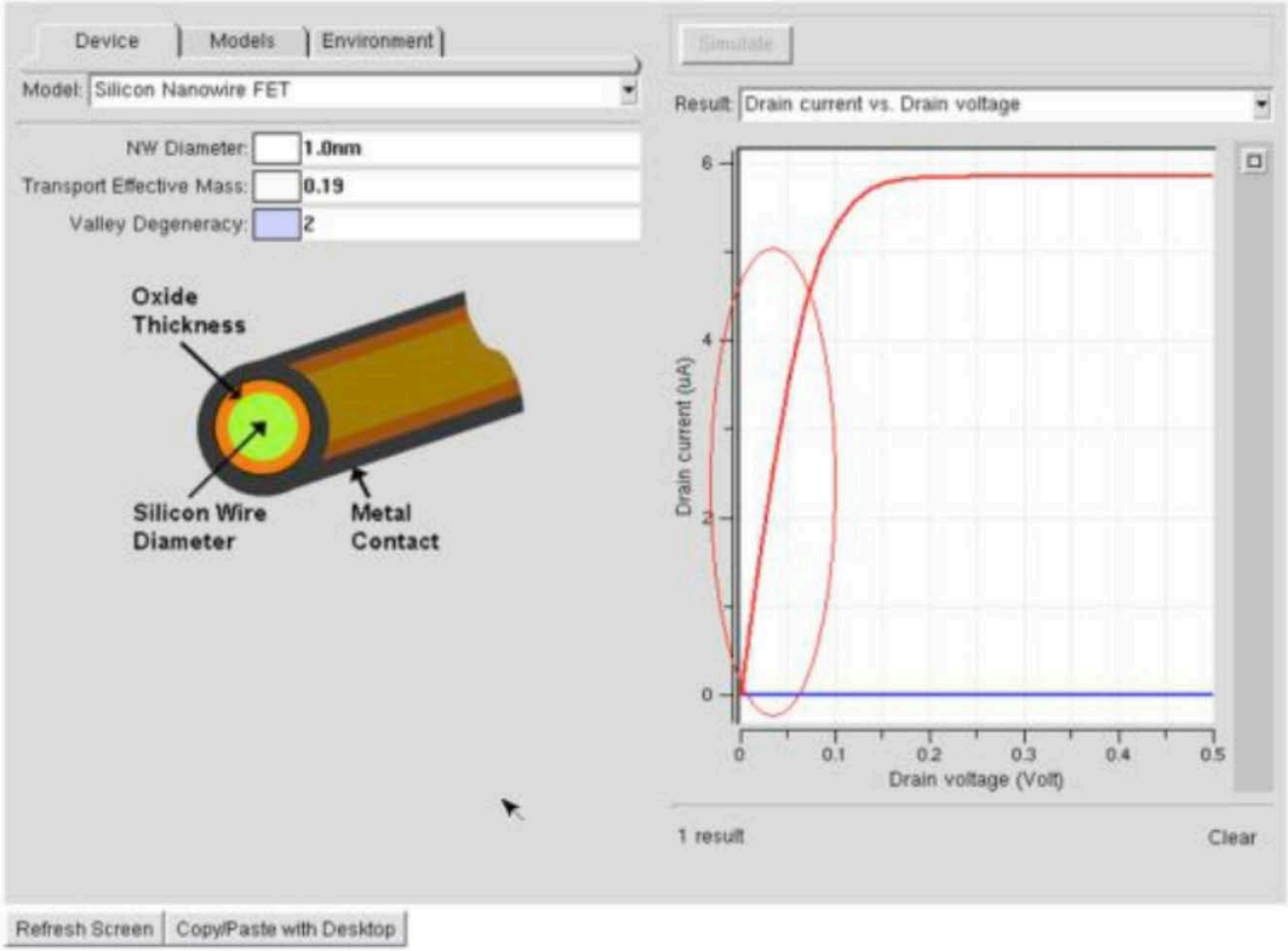
7a) Silicon Nanowire FET at 300K

Simulation Result:



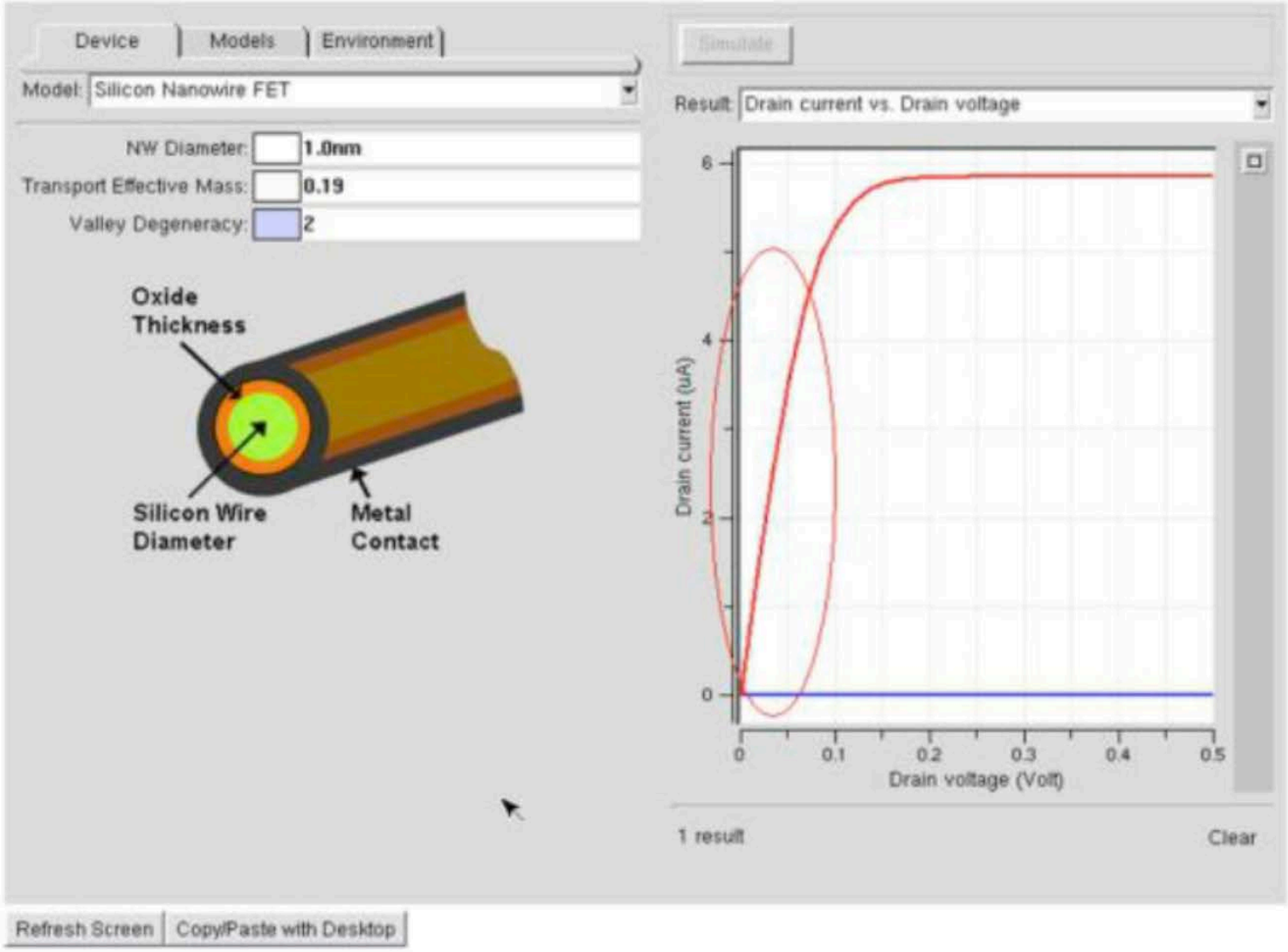
7a) Silicon Nanowire FET at 300K

Simulation Result: G_D = 5.89E-5siemens for V_G = 0.5V



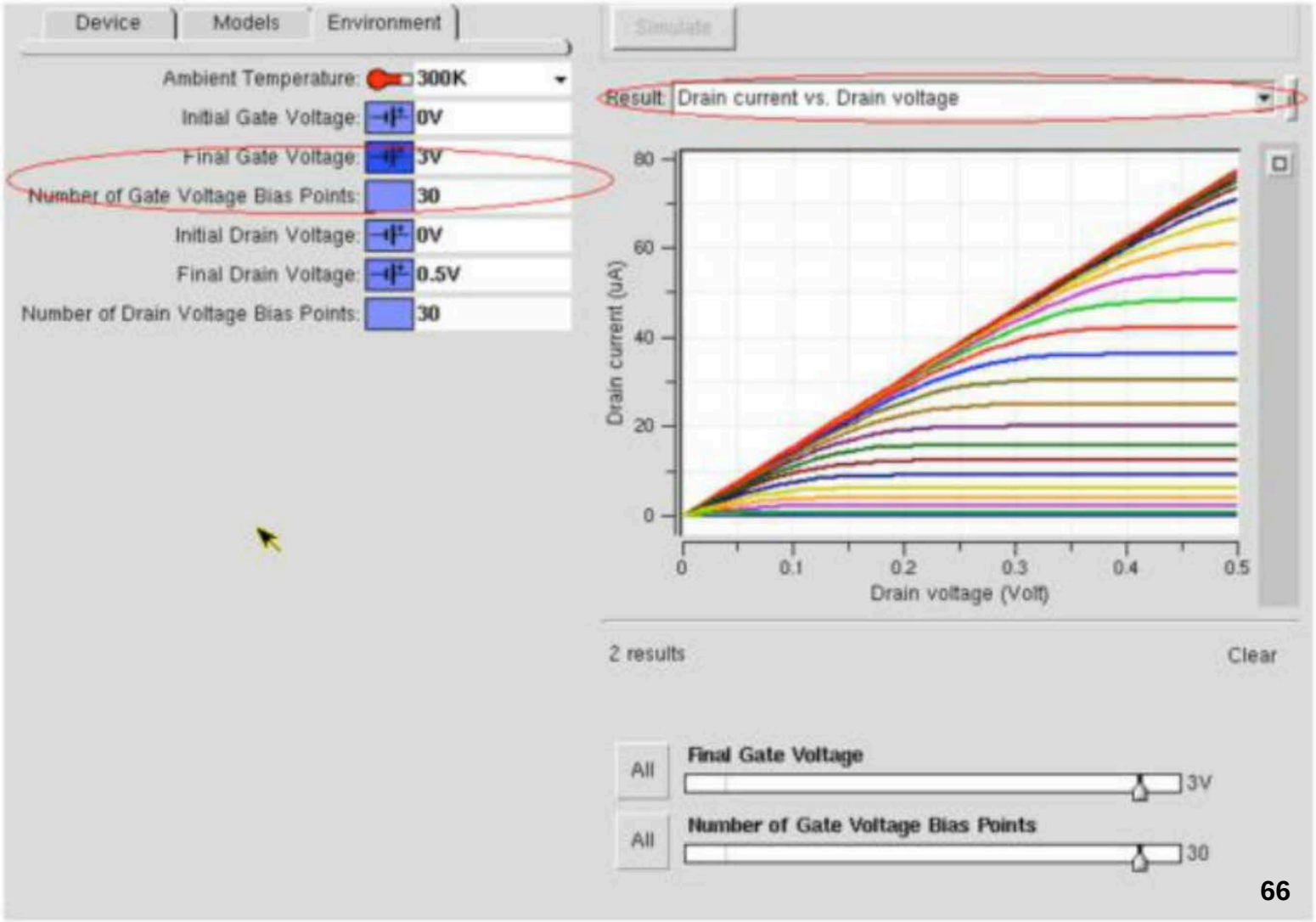
7a) Silicon Nanowire FET at 300K

Simulation Result: G_D = 5.89E-5siemens for V_G = 0.5V G_Q = 1.55E-4siemens



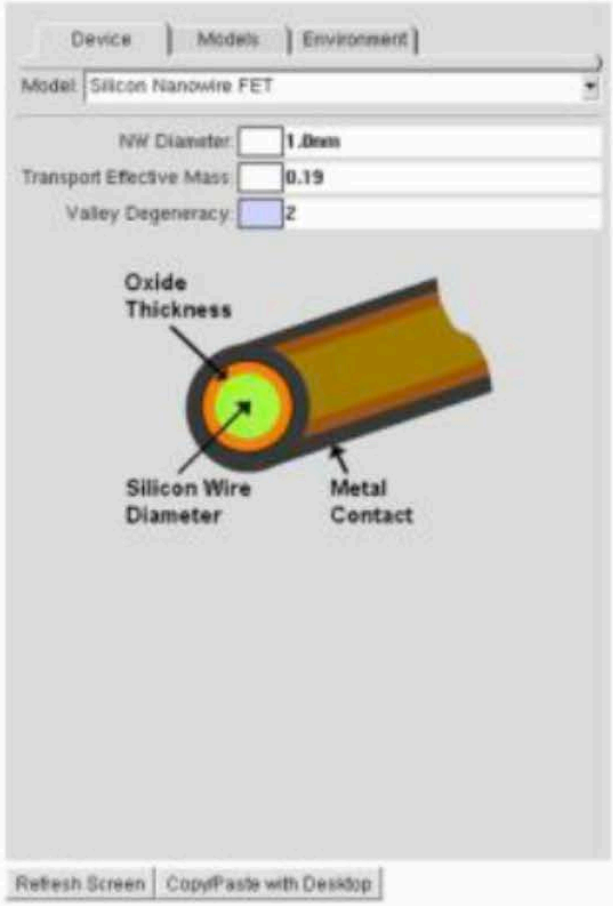
7a) Silicon Nanowire FET at 300K

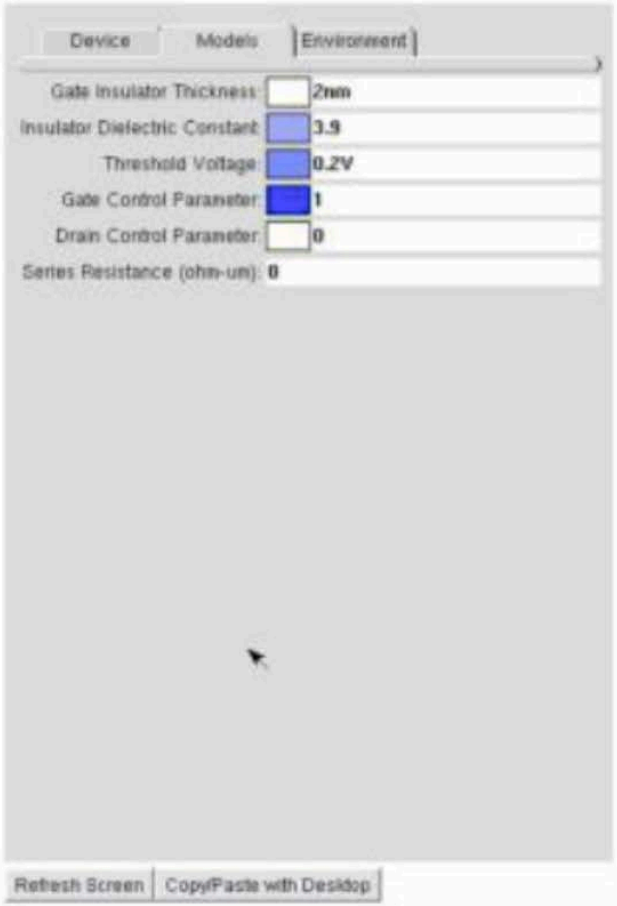
Simulation Results: G_D = 1.55E-4siemens at V_G > 1.5V G_Q = 1.55E-4siemens

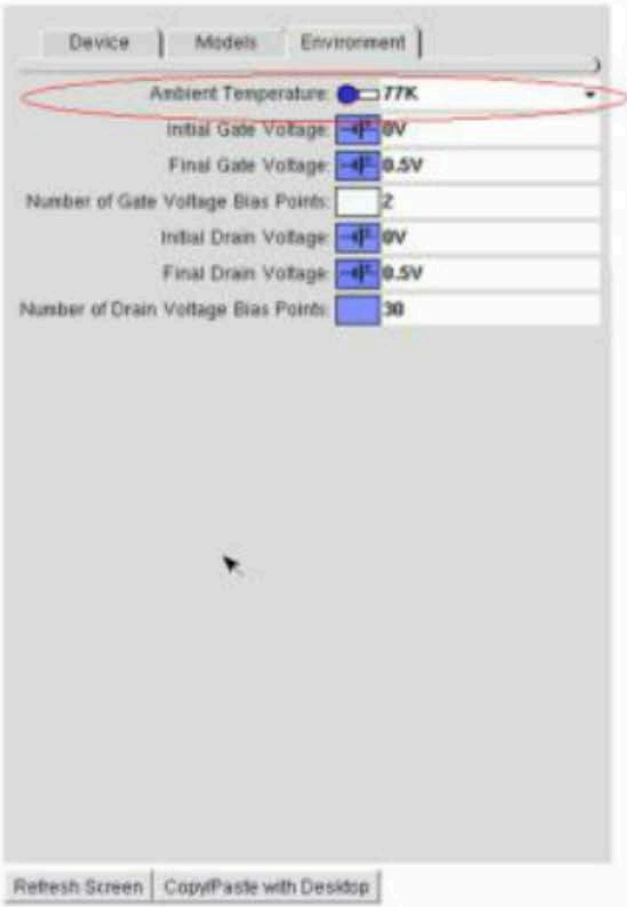


7b) Silicon Nanowire FET at 77K

Material Parameters and Settings:

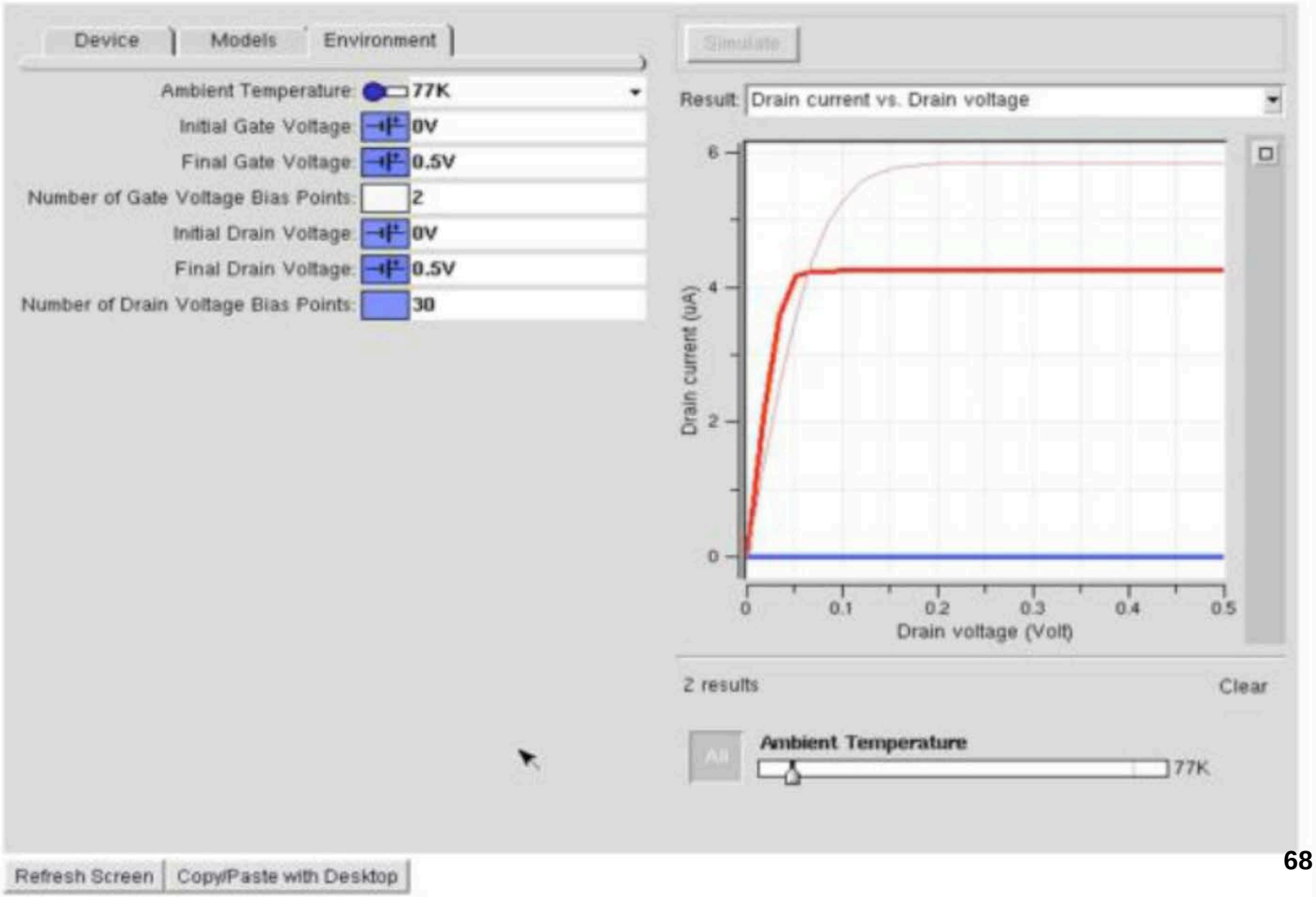






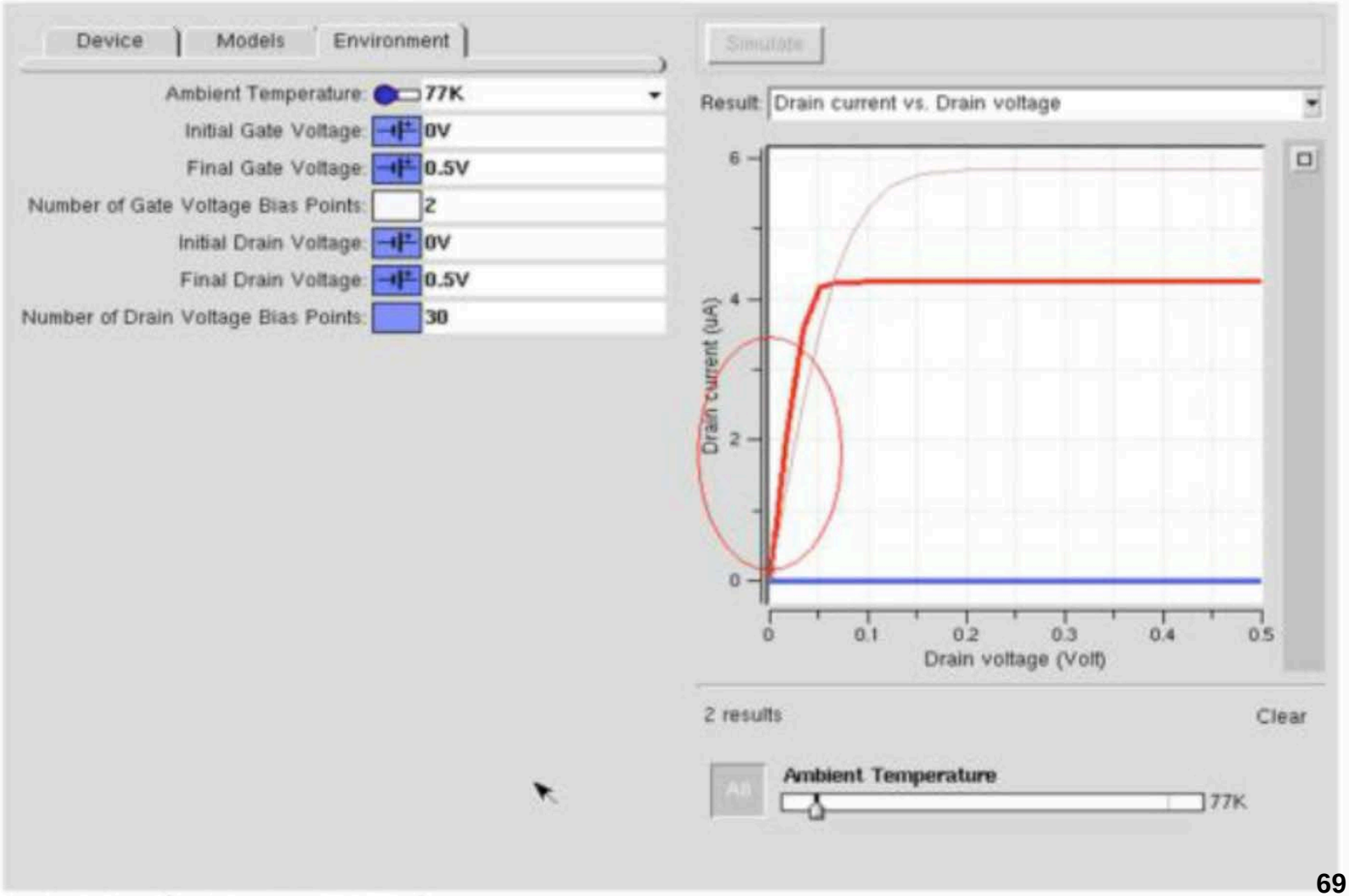
7b) Silicon Nanowire FET at 77K

Simulation Result:



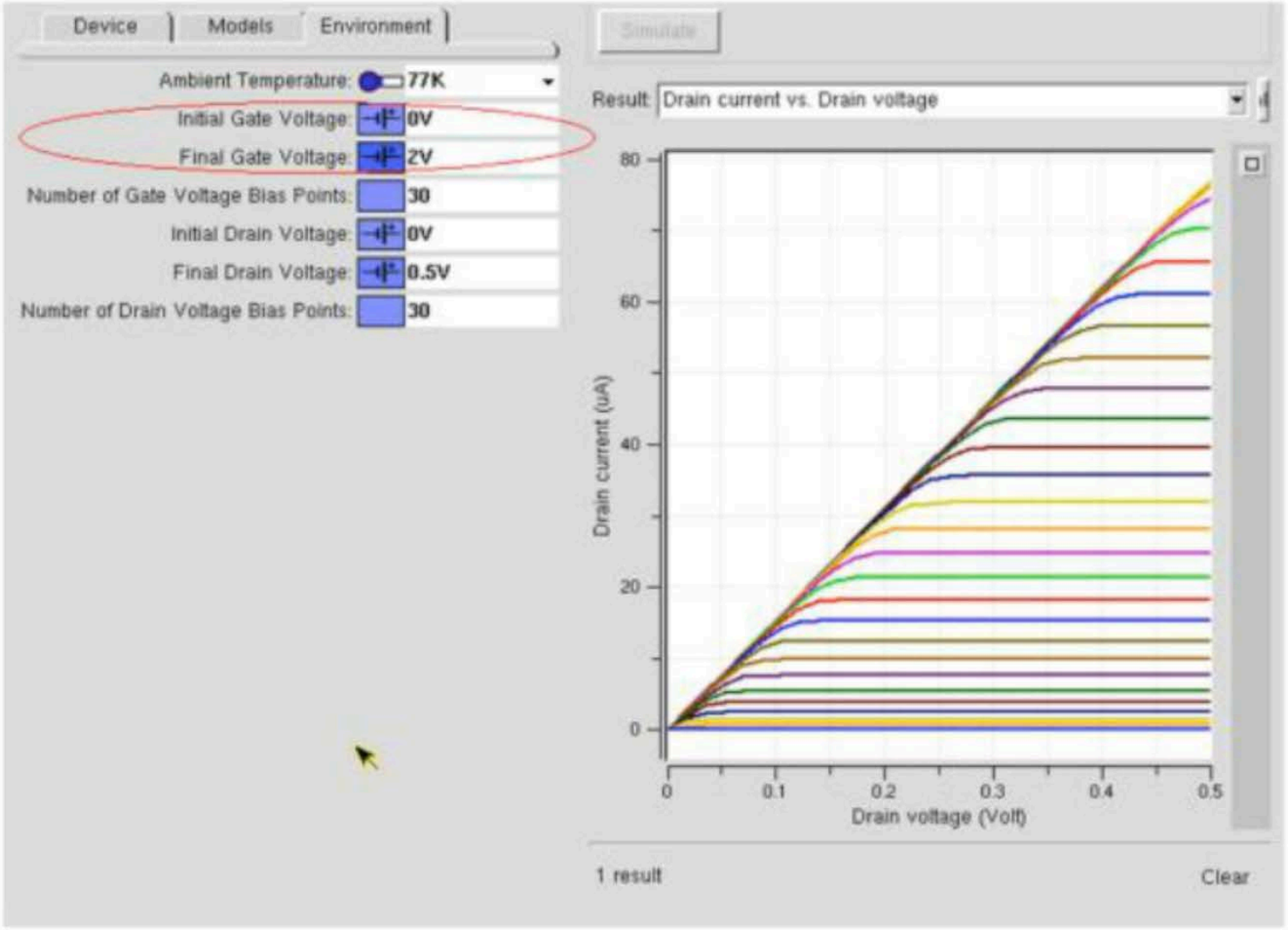
7b) Silicon Nanowire FET at 77K

Simulation Result: G_D = 8.84E-5siemens at V_G = 0.5V G_Q = 1.55E-4siemens



7b) Silicon Nanowire FET at 77K

Simulation Results: G_D = 1.55E-4siemens at V_G > .1V G_Q = 1.55E-4siemens



7b) Silicon Nanowire FET at 77K

Comparison of conventional MOSFET to Nanowire: Conductance vs. VGS

MOSFET:

As VG increases GC increases linearly:

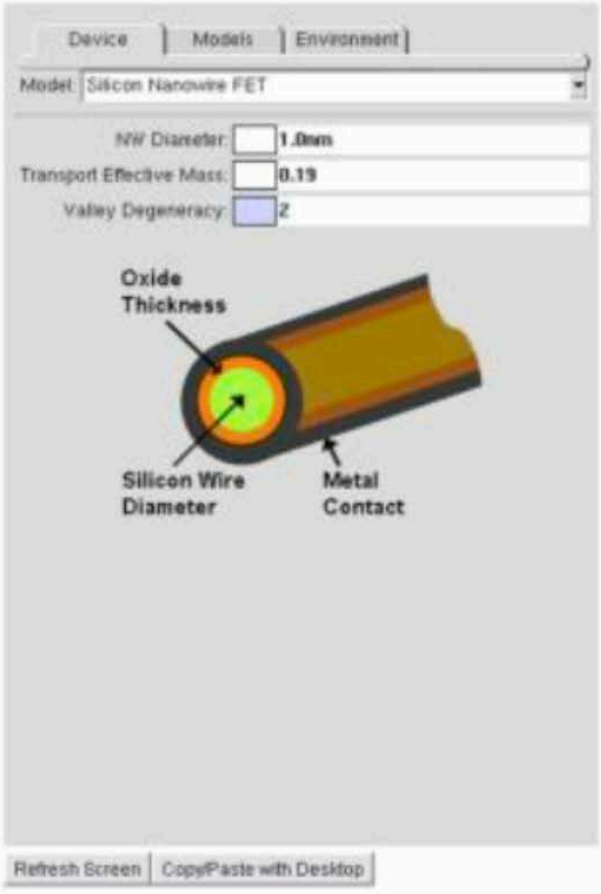
$$G_C = M \cdot \frac{2 \cdot q^2}{h}$$

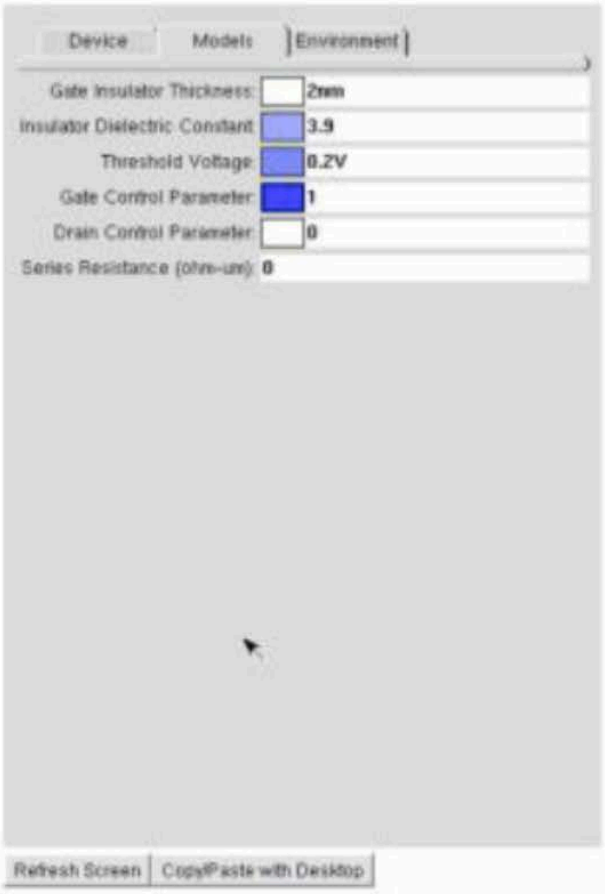
Nanowire FET:

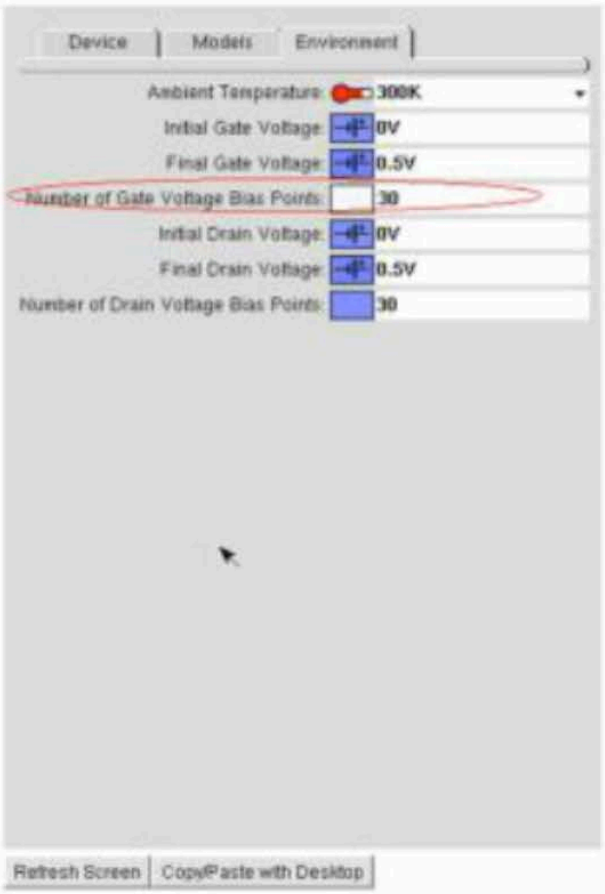
As VG increases GC increases in quantized steps

7c) Deducing Components of I_{ON}

Material Parameters and Settings:

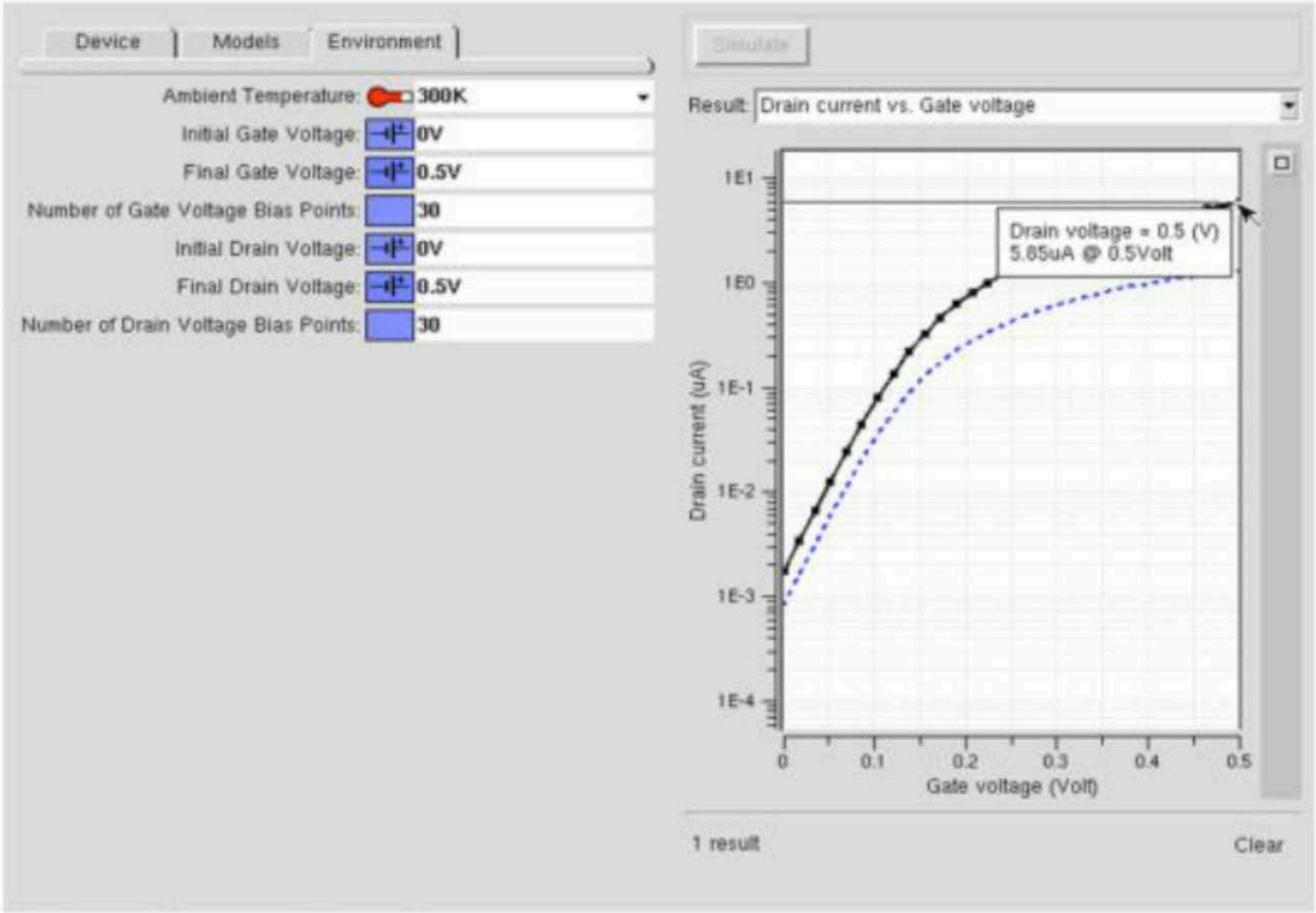






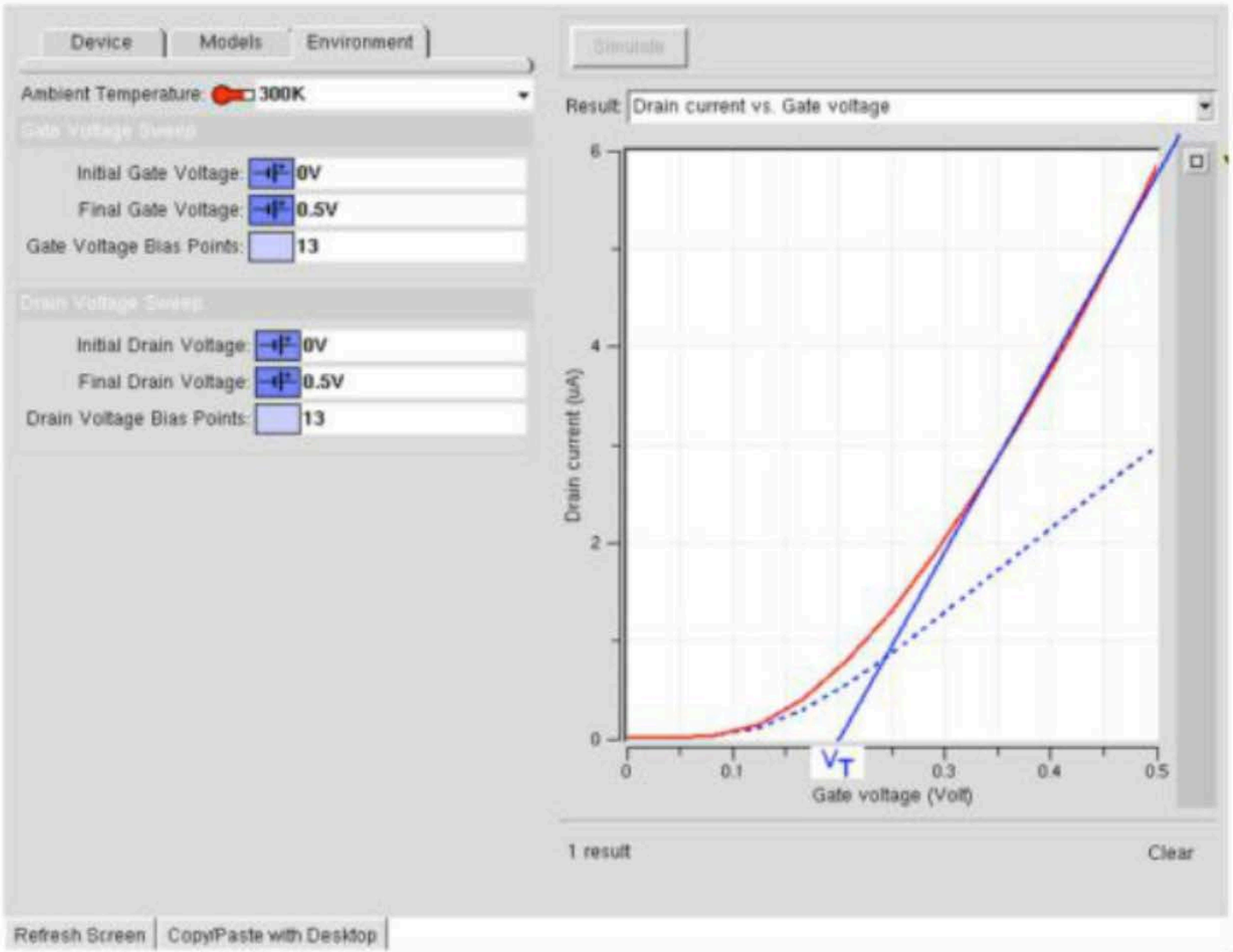
7c) Deducing Components of I_{ON}

Simulation Result: I_{ON} = 5.85uA



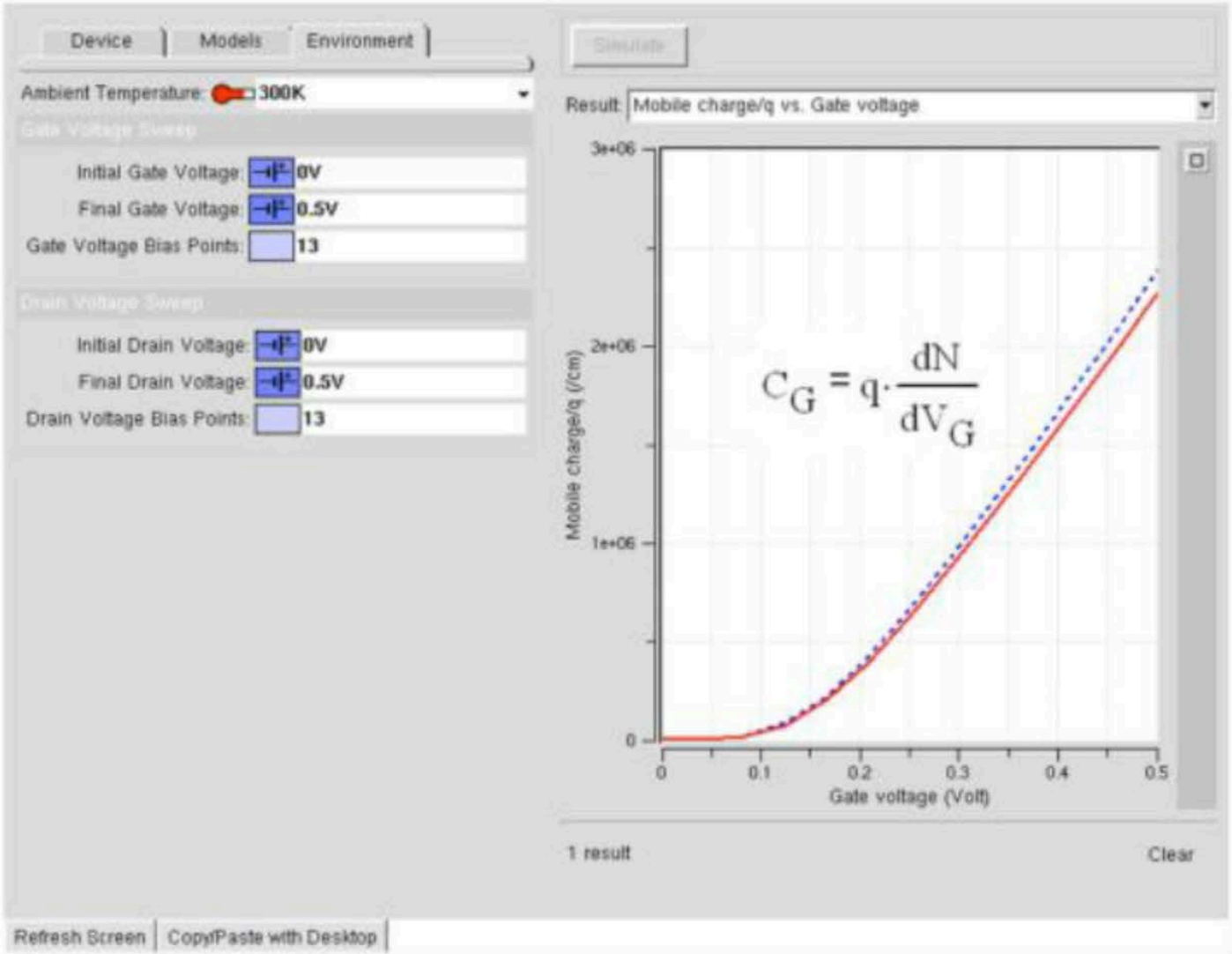
7c) Deducing Components of I_{ON}

Simulation Result: V_T = 0.2V



7c) Deducing Components of I_{ON}

Simulation Result: C_G = 1.09E-12F/cm



7c) Deducing Components of I_{ON}

$$\langle v(0) \rangle = \frac{I_{ON}}{C_G\left(V_G - V_T\right)}$$

$$\langle v(0) \rangle = 6.71E6 \frac{cm}{s}$$