High-Frequency Carbon Nanotube Transistors: Fabrication, Characterization, and Compact Modeling

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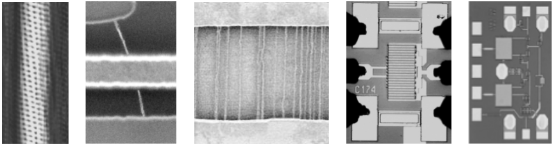
Motivation

Claims about CNTFETs

1. Analog HF applications are the most suitable entry point for CNTFETs
2. Device linearity is most valuable for analog HF applications!

Challenges

1. Provide access to intrinsic material properties in fabricated devices
2. Utilize CNTFETs for applications



From materials science to system engineering!

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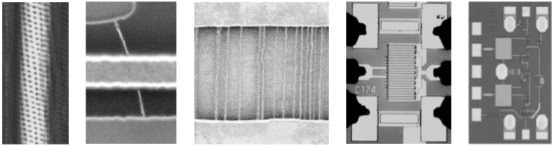

From materials science to system engineering!

Agenda

Content

- CNTFETs for analog HF applications?
- Challenges in designing and manufacturing CNTFETs
- Current status of CNTFET technology for HF applications
- CCAM – A compact model for HF CNTFETs
- Benchmark circuit design studies

Backup

- Trap induced apparent linearity of CNTFETs
- Why current physics-based compact models fail
- CCAM for designing analog and digital applications
- CVD and DEP-based CNTFET manufacturing - pros and cons

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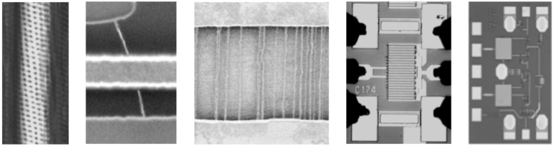
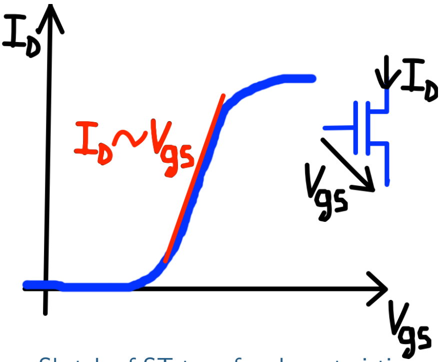
Introduction – Device linearity

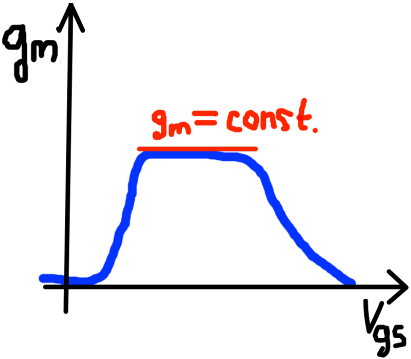


From materials science to system engineering!

Introduction - Device linearity

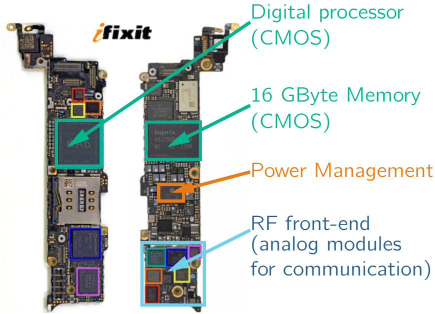


Sketch of ST transfer characteristic



Sketch of related transconductance

→ Device linearity is essential in communication systems!

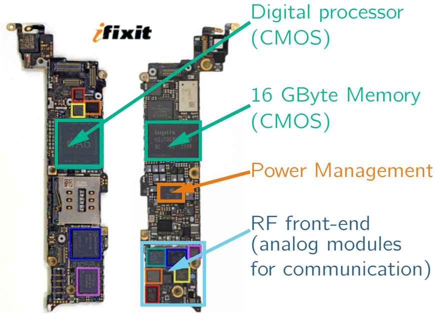


Circuit board of an Iphone 5

RF front-end:

- High volume and high-speed data transmission required
- Spectral efficiency (determined by signal distortion) of circuit components and transmission speed limited by e.g. circuit technology and available power (battery life time!)
- Device linearity could help to meet future communication demands

Electronics for mobile communication



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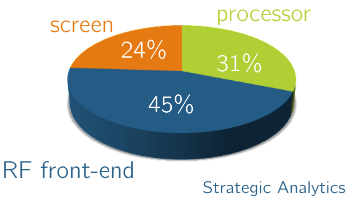

Power consumption breakdown

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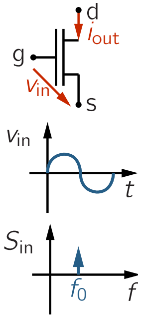
Example: Amplifier linearity at device level



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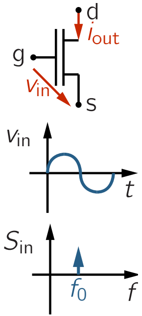
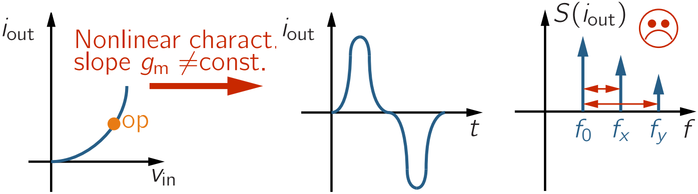


Conventional semiconductors (e.g. Si MOSFET)



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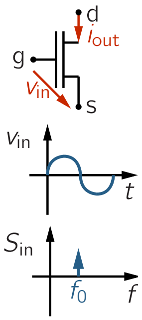

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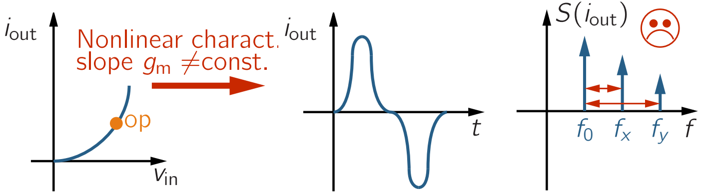
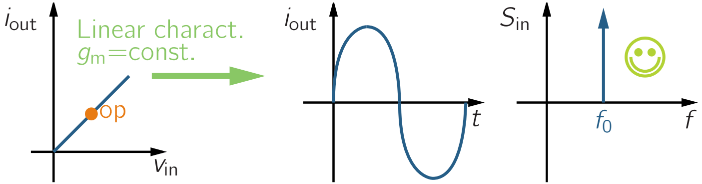


CNTFET technology



Linearity summary

Conventional seminconductors (e.g. silicon MOSFET)

- ☹ Signals distortion if output depends nonlinearly on input
- ☹ Interference with other channels
- ☹ Expensive filters required
- ☹ Higher losses and higher power consumption

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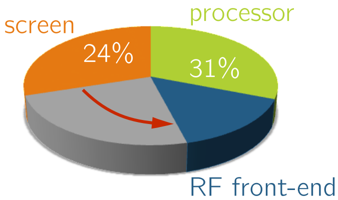
CNTFET technology

- ☺ Purer signals allow higher data rates
- ☺ Simpler systems $\rightarrow$ lower cost
- ☺ Lower power consumption (= longer battery life time)



Projected power consumption breakdown if linearity is exploited

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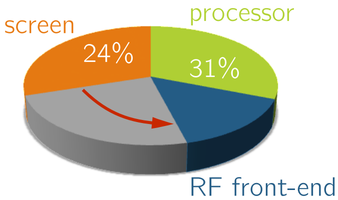


Projected power consumption breakdown if linearity is exploited

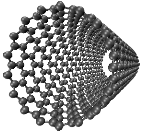
→ Distortion/ device linearity is a major issue in mobile communication!

Designing CNT transistors - Challenges

How to obtain and provide access to the unique intrinsic properties of CNTFETs and how to use them for applications?

Transistor properties affected by . . .

- intrinsic properties of semiconductor material
- channel morphology
- device architecture
- interface properties of the various material stacks



Intrinsic properties

Designing CNT transistors

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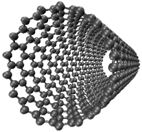

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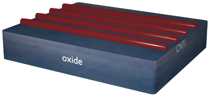

Channel morphology

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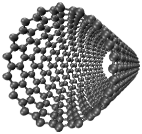

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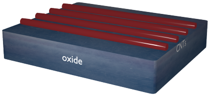
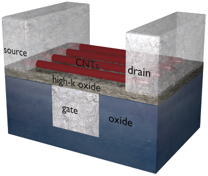


Channel morphology



Device architecture

Designing CNT transistors

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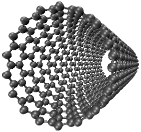

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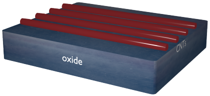

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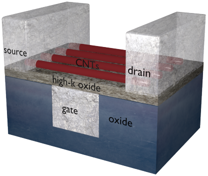

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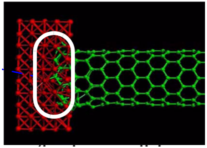
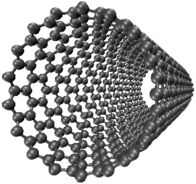


Interface properties

Selected unique intrinsic CNTFET properties

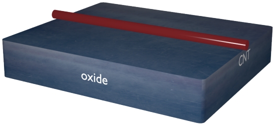
- Variable bandgap: $E_{\mathrm{gap}}(d_{\mathrm{cnt}}) = 0 \ldots 1.2\,\mathrm{eV}$ (i. e. semiconducting or metallic behavior)
- Typical: $d_{\mathrm{cnt}} \approx 0.5 \ldots 3\,\mathrm{nm}$
- One-dimensional carrier transport and density of states, i. e. low scattering probability
- High current carrying capability: $\approx 25\,\mu\mathrm{A}$
- Low intrinsic capacitances $\approx 1\,\mathrm{aF}$
- High carrier velocity up to Fermi velocity of Graphene ($\approx 1 \times 10^8\,\mathrm{cm\,s^{-1}}$)
- Linearity at device level (based on 1D transport)



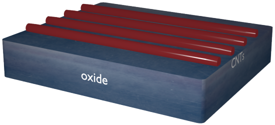
(17,0)-tube,
$d_{\mathrm{cnt}} \approx 1.3\,\mathrm{nm}$,
$E_{\mathrm{gap}} \approx 0.64\,\mathrm{eV}$,
l_{cnt} up to several mm

$\rightarrow$ Potential for high frequency applications with significantly reduced signal distortion

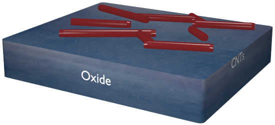
Channel morphology depends on the fabrication



Single tube channel
single CNT bridging S & D



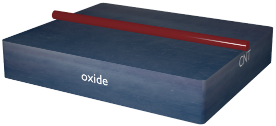
Multi tube channel
aligned CNTs bridging S & D



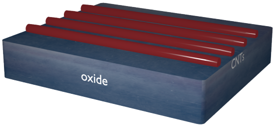
Thin film channel
Intercrossing CNT chains bridging S & D

- Typical methods: (*i*) CVD for in place growth, (*ii*) DEP deposition of pre-sorted CNTs, (*iii*) Polymer transfer of pre-grown CNTs
- Challenges depend on method (tube-placement, tube pre-sorting, tube length, catalysts for selective tube growth, contamination)
- Channel morphology determines channel resistance and current drive and thus the application

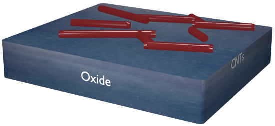
Channel morphology depends on the fabrication



Single tube channel
single CNT bridging S & D
Digital circuit applications



Multi tube channel
aligned CNTs bridging S & D
Analog high-frequency applications



Thin film channel
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Sensor applications

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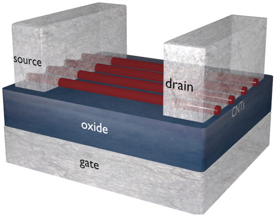
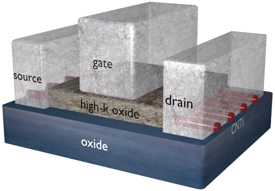


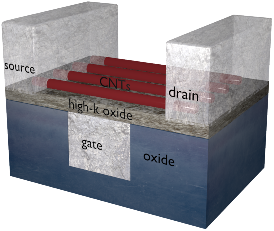
Global back gate CNTFET

Test structure and Sensor applications



Top gate CNTFET

Analog and digital applications



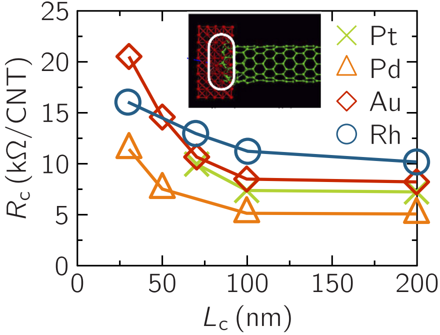
Local back gate CNTFET

Analog, digital and high performance sensor applications

- Electrode design and device structure determine gate control and parasitic capacitances!
- Channel down-scaling limited by lithographie
- Complexity limited available process modules and tools

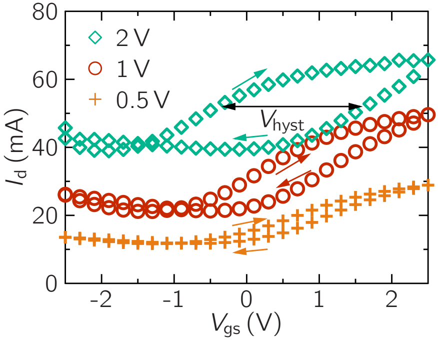
Interface properties affects device behavior

Contact resistance



Contact resistance for different metals and different contact length (exp. data) [1]

Oxide interface traps



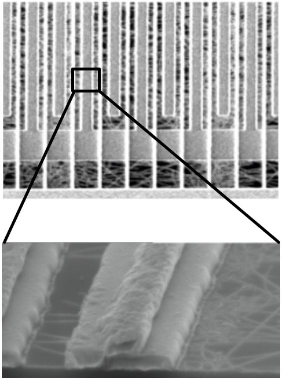
Experimental data of a forward and backward sweep [2]

- Find proper material for contacts (metall, carbon, . . .) to define the barrier (see later)
- High gate oxide quality and thoroughly wafer cleaning ensure low trap density

CNTFET technology status for analog HF applications

[3] – M. Schroter, M. Claus . . . , IEEE J. of the Electron Devices Society, 1(1), pp. 9–20, 2013.

Multi-tube CNTFETs



- high current, high power application (1000–3000 parallel tubes)
- scale with tube density, finger number and width to desired applications
- relaxed constraints for technology (800 nm channel length)
- parasitic metallic tubes in the channel (20%-30%)
- first prototyp technologies available ($f_{\mathrm{T,peak}} \approx 10\,\mathrm{GHz}$, $G_{\mathrm{power}} > 10\,\mathrm{dB}$)
- Note: Device linearity has experimentally not been proven so far

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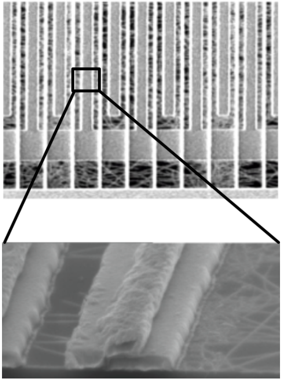

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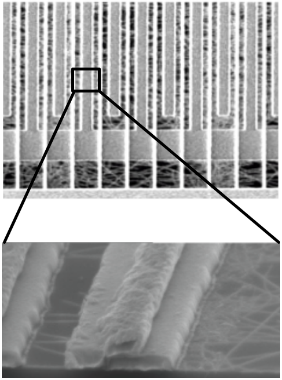

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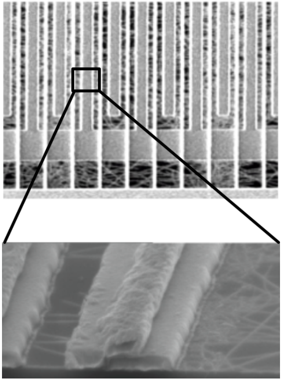

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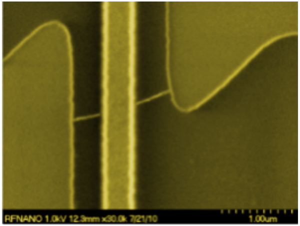
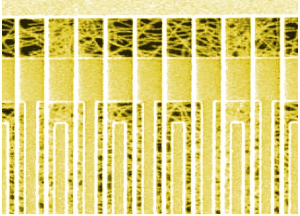
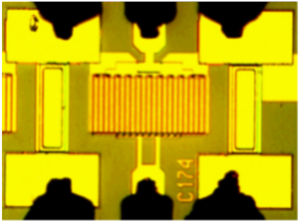
Status of HF CNTFET technology I



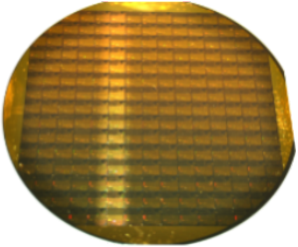
Single-tube CNTFET



Multi-tube Multi-finger CNTFET

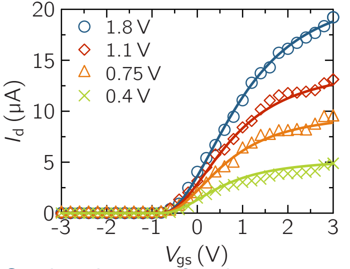


HF CNTFET in GSG configuration

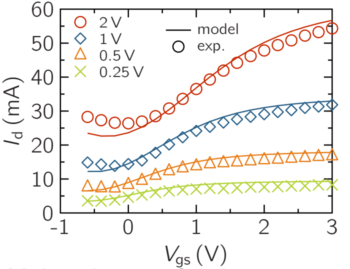


4 inch wafer

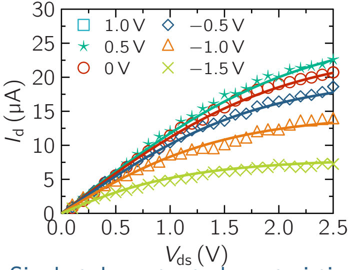
Status of HF CNTFET technology II



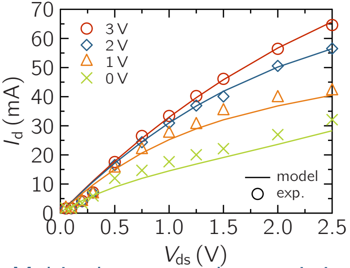
Single tube transfer characteristic



Multi tube transfer characteristic

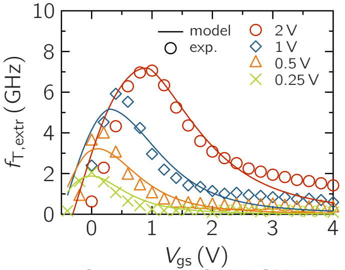


Single tube output characteristic

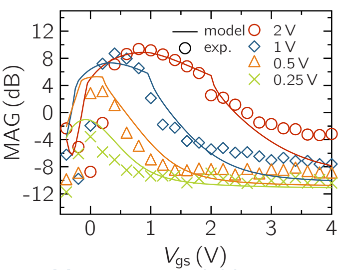


Multi tube output characteristic

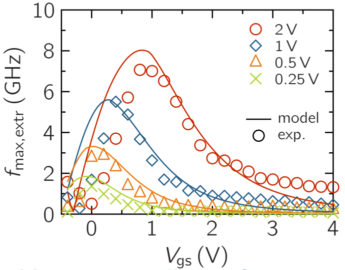
Status of HF CNTFET technology III



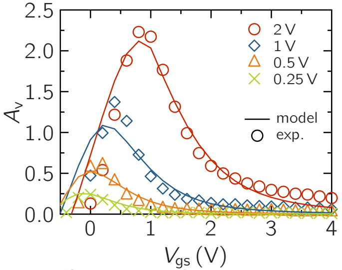
Transit frequency of HF CNTFET



Maximum available gain



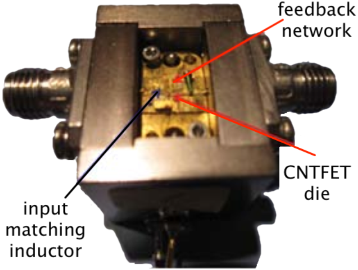
Maximum oscillation frequency

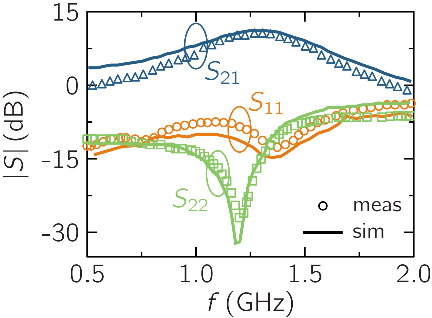


Intrinsic voltage gain

First circuit results - L-band RF amplifier

- First CNT-based single-stage L-band RF amplifier [4]
- 11 dB linear gain with 10 dB input/output return loss at 1.3 GHz





- Analog HF applications are most suitable entry point for CNTFETs!
- Already possible with existing fabrication methods
- Device linearity is most valuable for analog HF applications – but has experimentally not been proven so far

CCAM – A compact model for HF CNTFETs

[5] – M. Claus, et al., Workshop on Compact modeling, Vol. 2, pp. 770-775, 2012.
[6] – M. Schroter, . . . M. Claus, IEEE Transactions on Electron Devices, 2014.

Compact models for HF CNTFETs I

Purpose

- allows circuit design, simulation and optimization for an existing technology
- understanding of circuit properties and their relation to CNTFET technology
- prediction/ extrapolation of circuit and system properties for future technology nodes (with less imperfections or scaled dimensions)
- feedback for technology development: which technology parameters needs to be improved to boost circuit performance

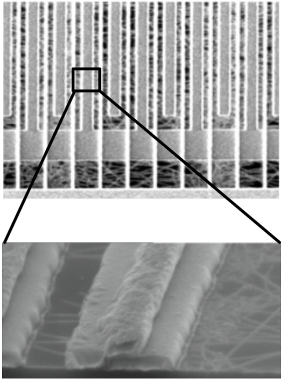
State-of-the-art of CNTFET compact models

- main focus on digital applications ("beyond CMOS")
  $\rightarrow$ nanoscale channel lengths
- models mostly restricted to single-tube CNTFETs and low voltages
- formulations focus mostly on describing DC behavior
- almost no experimental verification of model formulations

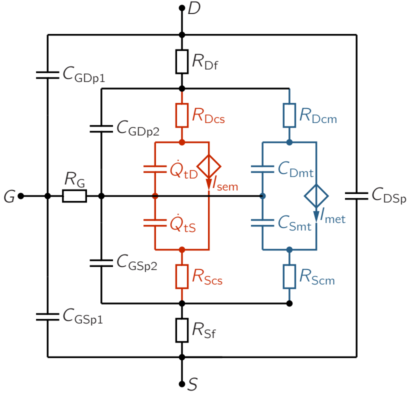
$\rightarrow$ little emphasis on multi-tube high-frequency (HF) analog applications

Compact models for HF CNTFETs III

- CM for MT CNTFETs includes: equivalent circuit for semiconducting tubes + metallic tubes + parasitic elements



Multi-tube CNTFET



Equivalent circuit

Compact modeling issues

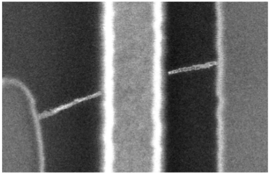
- All fabricated transistors have Schottky-like barriers (SB) between metal contacts and CNT

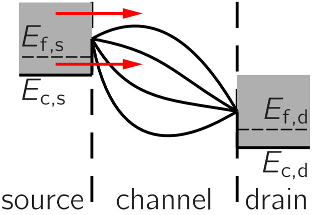
→ compact modeling very difficult

→ no feasible physics-based approach (for current and charge) is known

→ almost all existing compact models do not consider SB properly (compared to experiments)

Two parallel approaches in our group: semi-physics based (CCAM) and physics-based (TCAM) compact model



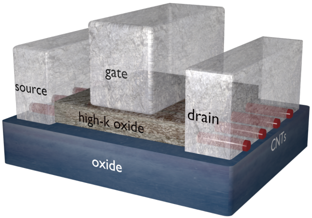


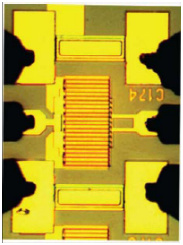
Compact model: CCAM

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. XX, NO. XX, XX XX

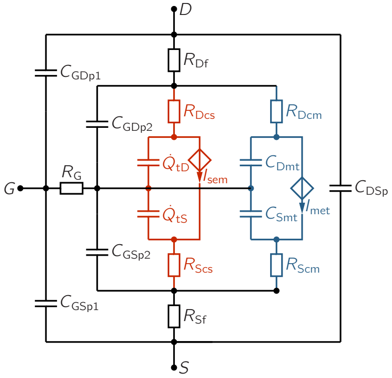
A semi-physical large-signal compact carbon nanotube FET model for analog RF applications

M. Schröter, *Senior Member, IEEE*, M. Haferlach, A. Pacheco, S. Mothes, P. Sakalas, *Member, IEEE* and M.Claus





Compact model: CCAM



Equivalent circuit of the compact model

CCAM Features

- bias-dependent formulation for internal elements (i. e. large signal model)
- temperature and geometry dependence for all equivalent circuit elements
- access to technology parameters e. g. fraction of metallic tubes
- noise and trap model

- CCAM has been implemented in Matlab and Verilog-A, making it widely available across circuit simulators
- make use of HICUM infrastructure for developing and maintaining industry standard model

CCAM equations (not showing all)

- Drain current:

$$I_{\mathrm{sem}} = I_{\mathrm{DS0}} f_{\mathrm{GS}} f_{\mathrm{DS}}$$

- GS depdendence:

$$f_{\mathrm{GS}} = \left(\frac{u_{\mathrm{GS}} + \sqrt{u_{\mathrm{gs}}^2 + a_{\mathrm{thg}}}}{1 + \sqrt{1 + a_{\mathrm{thg}}}} \right)^2 \left(1 + 2 \frac{1 + u_{\mathrm{GS}}}{\sqrt{u_{\mathrm{GS}}^2 + a_{\mathrm{thg}}}} \right)$$

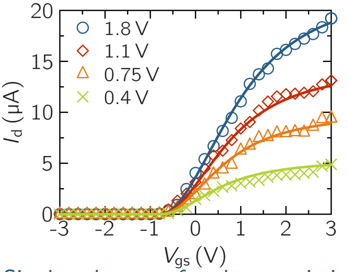
with $u_{\mathrm{GS}} = 1 - V_{\mathrm{thg0}} / v_{\mathrm{gt}}$, $v_{\mathrm{gt}} = V_{\mathrm{GS}} - V_{\mathrm{fb}}$

- DS dependece (simple form for scattering):

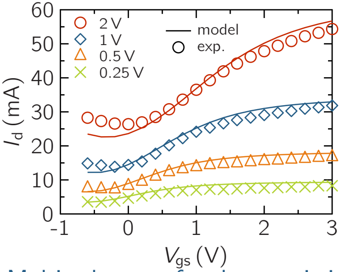
$$f_{\mathrm{DS}} = u_{\mathrm{DS}} \left(1 + |u_{\mathrm{DS}}|^{\beta} \right)^{-1/\beta}$$

- Similar smoothing functions for the charge

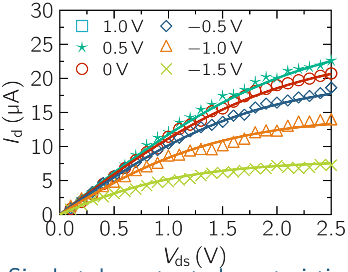
Experimental verification I



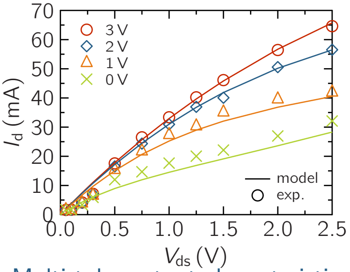
Single tube transfer characteristic



Multi tube transfer characteristic

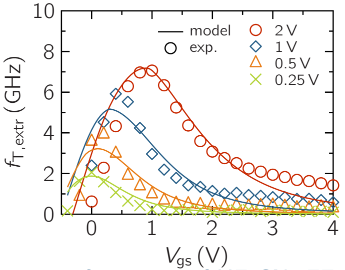


Single tube output characteristic

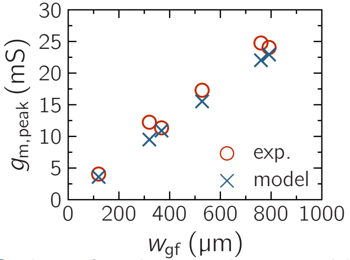


Multi tube output characteristic

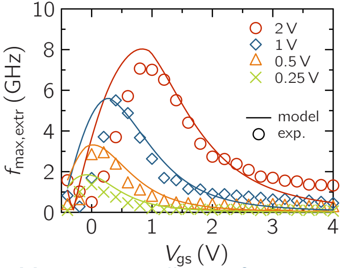
Experimental verification II



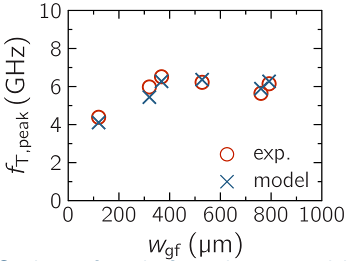
Transit frequency of HF CNTFET



Scaling of peak g_m with gate width



Maximum oscillation frequency



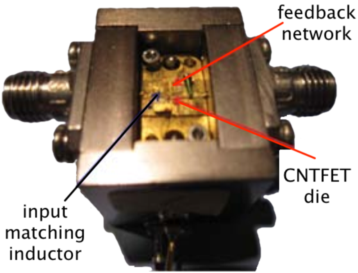
Scaling of peak f_T with gate width

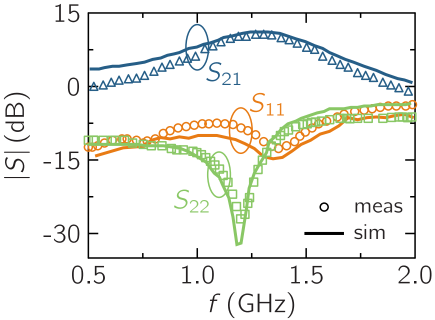
Benchmark circuit design studies

[7] – M. Claus, et al., IMOC, 2013.

Circuit results - L-band RF amplifier

- First CNT-based single-stage L-band RF amplifier [4]
- 11 dB linear gain with 10 dB input/output return loss at 1.3 GHz

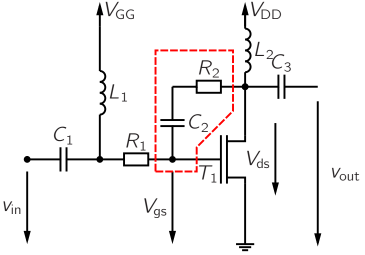




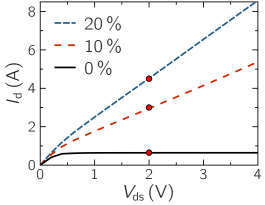
- Good comparison between experimental results and model

Circuit results - Power amplifier

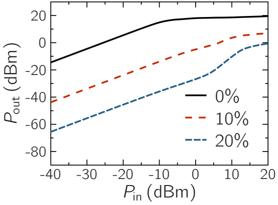
- Class-A power amplifier designed at $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$ (low saturation voltage) and $V_{\mathrm{ds}} = 2\,\mathrm{V}$ for 2 GHz applications
- 150 similar devices are connected in parallel to have an output power of 16 dBm



PA circuit with matching and stabilization subcircuits



Output characteristic for various m_{frac}

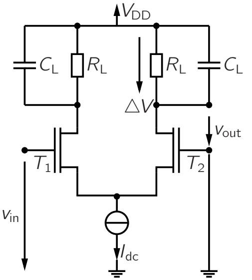


Output power vs input power for various m_{frac}

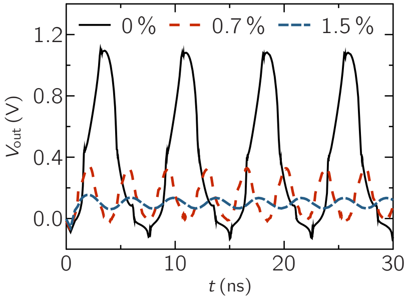
- Power gain only for less than 10 % metallic tube fraction

Circuit results - Ring oscillator

- Ring oscillator (RO) build up in current mode logic (CML)
- Differential architecture, CML building block acts like an inverter



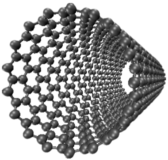
CML building block



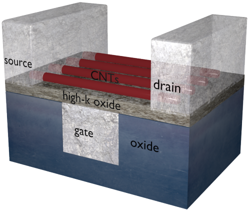
Output voltage oscillation for various m_{frac}

- Device gradually losses its basic ON/OFF switching properties
- Oscillation only for $m_{\mathrm{frac}} < 2\,\%$
- RO is much more sensitive to m_{frac} than the PA

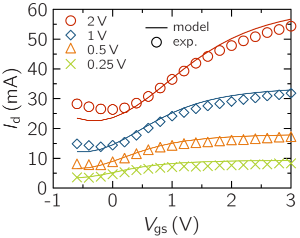
Summary



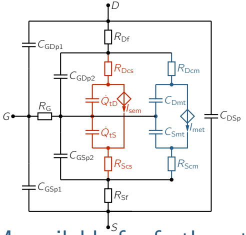
Unique intrinsic electrical properties



Great potential for HF and low distortion applications



Parasitic metallic tubes most severe issue



CCAM available for further studies

References I

[1] A. D. Franklin, D. B. Farmer, and W. Haensch, "Defining and overcoming the contact resistance challenge in scaled carbon nanotube transistors," *ACS Nano*, vol. 8, no. 7, pp. 7333–7339, 2014.

[2] M. Haferlach, M. Claus, T. Nardmann, A. Pacheco-Sanchez, P. Sakalas, and M. Schröter, "Trap-induced apparent linearity of cntfets (invited)," in *Nanotech, Workshop on Compact Modeling (WCM)*, 2014.

[3] M. Schroter, M. Claus, P. Sakalas, M. Haferlach, and D. Wang, "Carbon Nanotube FET Technology for Radio-Frequency Electronics: State-of-the-Art Overview (invited)," *IEEE Journal of the Electron Devices Society*, vol. 1, no. 1, pp. 9–20, 2013.

[4] M. Eron, S. Lin, D. Wang, M. Schroter, and P. Kempf, "An L-band carbon nanotube transistor amplifier," *Electronics Letters*, vol. 47, no. 4, pp. 265–266, 2011.

[5] M. Claus, D. Gross, M. Haferlach, and M. Schröter, "Critical review of cntfet compact models," in *NSTI-Nanotech (Workshop on Compact modeling)*, vol. 2, 2012, pp. 770–775.

[6] M. Schroter, M. Haferlach, A. Pacheco, S. Mothes, P. Sakalas, and M. Claus, "A semi-physical large-signal compact carbon nanotube fet model for analog rf applications (accepted)," *IEEE Transactions on Electron Devices*, 2014.

[7] M. Claus, A. Mukherjee, A. Moroguma, A. Pacheco, S. Blawid, and M. Schröter, "High-frequency benchmark circuit design for a sub 50 nm cntfet technology," in *SBMO/IEEE MTT-S International Microwave & Optoelectronics Conference (IMOC)*, 2013, pp. 1–5.