**Test for MOSFET Lab**

**(**[**http://nanohub.org/resources/mosfet**](http://nanohub.org/tools/mosfet)**)**

Note: only one choice is correct

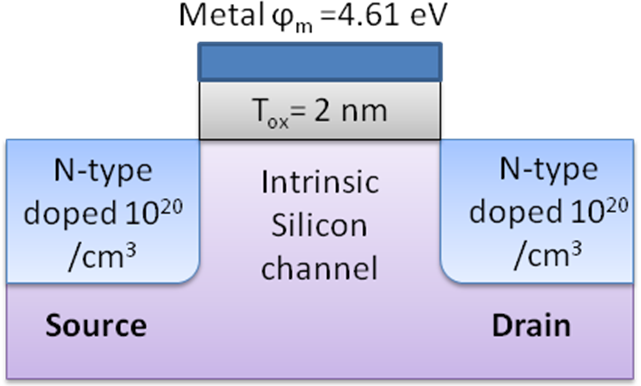
1. What does MOS stand for?
   1. Metal-Oxide-Silicon
   2. Metal-Oxide-Semiconductor
   3. Metal-On-Silicon
2. Match the correct pairs for different modes of operation of a MOSFET.

(X) Cut-Off or subthreshold (A) VGS> Vth; VDS < VGS-Vth

(Y) Linear or ohmic mode (B) VGS< Vth

(Z) Saturation or active mode (C) VGS> Vth; VDS > VGS-Vth

1. (X)-(B) , (Y)-(A), (Z)-(C)
2. (X)-(A) , (Y)-(B), (Z)-(C)
3. (X)-(C) , (Y)-(B), (Z)-(A)
4. What is true about the following Figure 1 (Assume a long channel length),



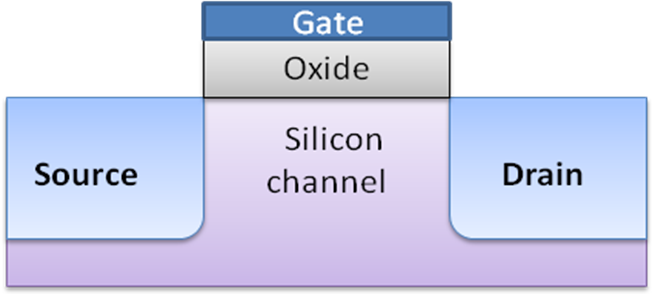
Figure

* 1. N-type MOSFET
  2. P-type MOSFET
  3. Can work as both N-type and P-type MOSFETs

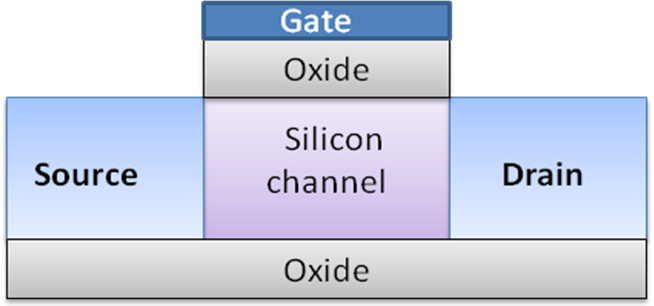
1. What is the threshold voltage for the MOSFET in Figure 1?
   1. 0.56 V
   2. 1.12 V
   3. 0 V
2. What will be the threshold voltage if Metal is replaced with N-Poly?
   1. 0.56 V
   2. 1.12 V
   3. 0 V
3. What is the best case for increasing the ON state current of device in Figure 1?
   1. Make thicker oxide.
   2. Replace metal with N-poly gate.
   3. Replace channel material with GaAs
4. What happens if we reduce channel length?
   1. Subthreshold slope ↓; DIBL ↑
   2. Subthreshold slope ↓; DIBL ↓
   3. Subthreshold slope ↑; DIBL ↑
5. What is the ideal sub threshold slope at room temperature?
   1. 100 mV/dec
   2. 60 mV/dec
   3. 25 mV/dec
6. A Silicon based NMOS has W=10µm and L=100µm and Bulk mobility, µn=600 cm2/V.s. What should be device dimension for the PMOS (µp=300 cm2/V.s) to have same ON state current.
   1. W=10µm ; L=50µm
   2. W=50µm ; L=200µm
   3. W=10µm ; L=100µm
7. Which of the following will lead to higher transconductance gm?
   1. Reducing oxide thickness
   2. Increasing channel length
   3. Reducing mobility
8. By what factor should the following parameters be multiplied while reducing MOSFET channel length by a factor β and keeping the same electric field within the device?

|  |  |  |  |
| --- | --- | --- | --- |
|  | Oxide thickness | Width | Drain bias |
|  | β | β | 1/β |
|  | 1 | 1/β | β |
|  | 1/β | 1/β | 1/β |

1. What is the typical thickness of inversion layer formed below oxide?
   1. 0.1 nm
   2. 2 nm
   3. 10 nm
2. Under what condition would punchthrough happen?
   1. Thickness, tox→ 0
   2. Length, Lchannel→ 0
   3. Doping Na → 0
3. Which of the following is not a short channel effect?
   1. Punchthrough
   2. Reducing subthreshold slope
   3. Increasing DIBL
4. Which of the following MOSFET device would have least sub threshold slope?
   1. Bulk MOSFET



* 1. UTB MOSFET



* 1. Double Gate MOSFET

