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MOS Capacitors: Theory and Modeling

1. Introduction
2. MOS Capacitor Electrostatics
   A. Delta-Depletion Approximation
   B. Exact Analytical Model
3. Ideal MOS Capacitor Capacitance
4. Deviations from the Ideal Model

Dragica Vasileska, ASU

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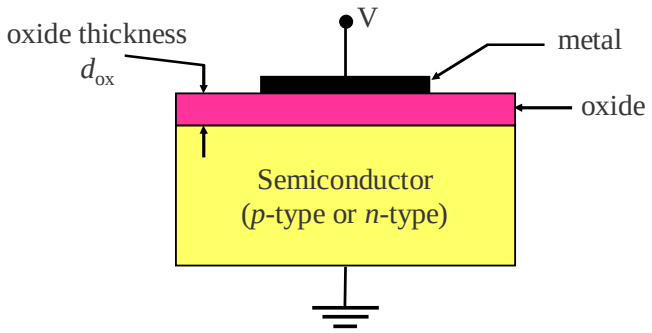
1. Introduction

- The Si MOSFET is the most important solid-state device for modern electronics. To understand its operation, we first need to understand the MOS capacitors:



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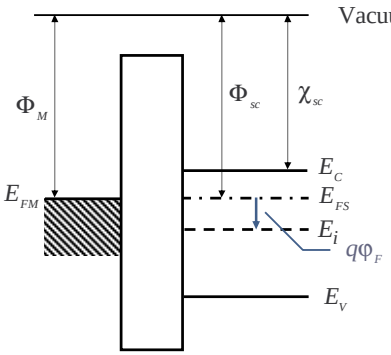
Energy-band diagram of IDEAL MOS capacitor

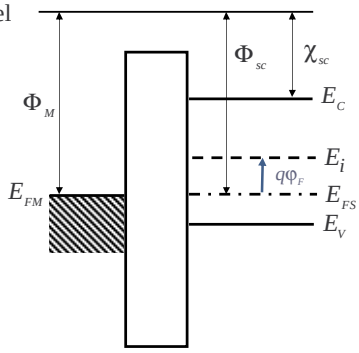
$$\Phi_M = \Phi_{sc}$$

n-type semiconductor



$$\Phi_M = \chi_{sc} + \frac{E_g}{2} - |q\varphi_F|$$

p-type semiconductor



$$\Phi_M = \chi_{sc} + \frac{E_g}{2} + q\varphi_F$$

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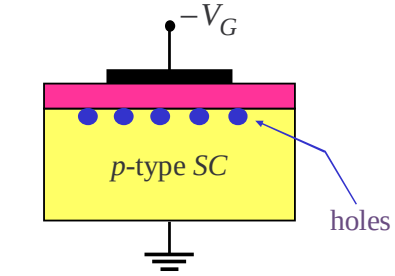
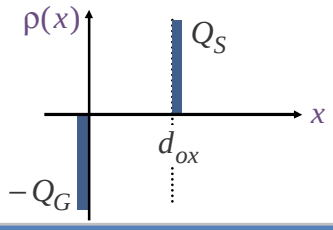
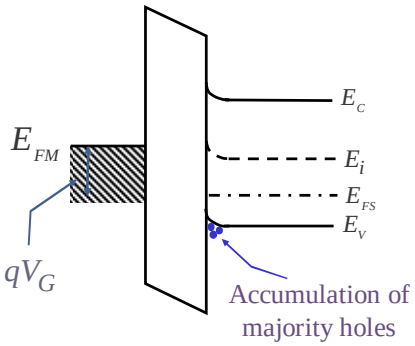
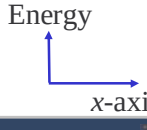
Accumulation

- Ideal MOS capacitor under **accumulation** bias conditions:









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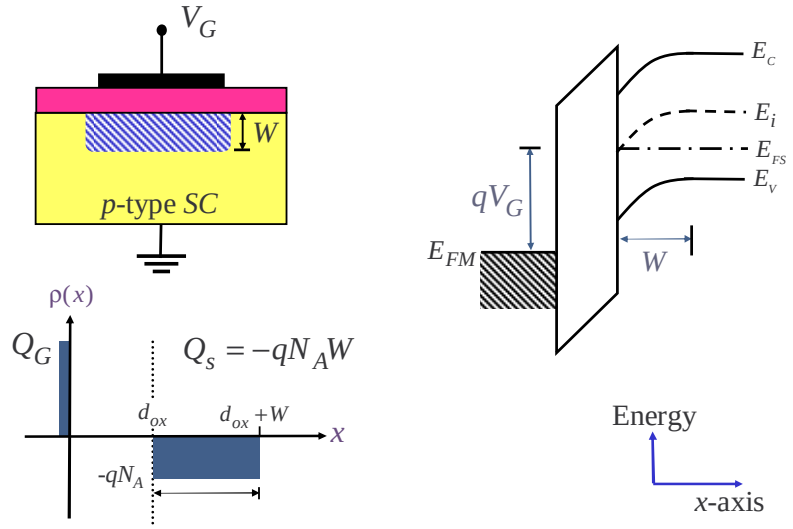
Depletion

- Ideal MOS capacitor under **depletion** bias conditions:



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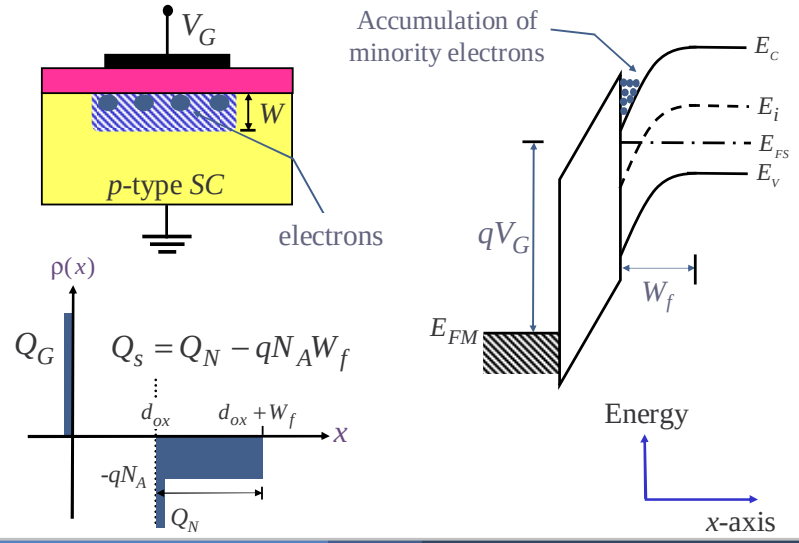
Inversion

- Ideal MOS capacitor under **inversion** bias conditions:



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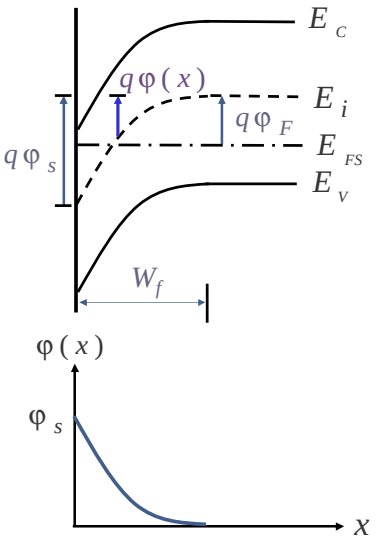
Terminology



(a) Bulk potential:

$$q\varphi_F = E_i(bulk) - E_{FS}$$

p-type SC: $\varphi_F = \frac{k_B T}{q}\ln\left(\frac{N_A}{n_i}\right) > 0$

n-type SC: $\varphi_F = -\frac{k_B T}{q}\ln\left(\frac{N_D}{n_i}\right) < 0$

(b) Potential:

$$q\varphi(x) = E_i(bulk) - E_i(x)$$

(c) Surface potential:

$$q\varphi_s = E_i(bulk) - E_i(0)$$

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Regions of operation

- Regions of operation for MOS capacitor with *p*-type SC:
  - (a) accumulation: $\varphi_s < 0$
  - (b) depletion: $0 < \varphi_s < 2\varphi_F$
  - (c) inversion: $\varphi_s \geq 2\varphi_F$
- The condition $\varphi_s = 2\varphi_F$ is called **onset of inversion**:

$$\left.\begin{aligned} n_s &= n_i \exp\left[\frac{E_{FS} - E_i(0)}{k_B T}\right] = n_i \exp\left(\frac{q\varphi_F}{k_B T}\right) \\ p_s &= n_i \exp\left[\frac{E_i(0) - E_{FS}}{k_B T}\right] = n_i \exp\left(-\frac{q\varphi_F}{k_B T}\right) \end{aligned}\right\} \rightarrow \begin{cases} n_s = p(bulk) \\ n_s p_s = n_i^2 \end{cases}$$

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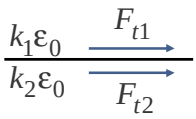
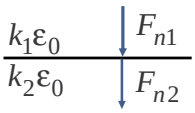
Fields and dielectrics

Tangential components



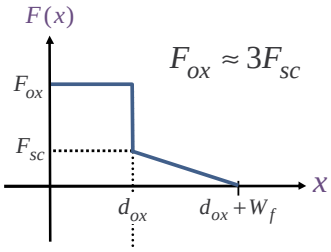
$$F_{t1} = F_{t2}$$

Normal components



$$D_{n1} = D_{n2}$$
$$k_1\varepsilon_0 F_{n1} = k_2\varepsilon_0 F_{n2}$$

- Electric field profile for a MOS capacitor with *p*-type SC under depletion condition:



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2. MOS Capacitor Electrostatics

- The potential distribution (profile) in the semiconductor side of a MOS capacitor is described with the 1D Poisson equation:

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{k_s\varepsilon_0}$$

where the space charge density is given by:

$$\rho(x) = q\left(p - n + N_D^+ - N_A^-\right)$$

- The 1D Poisson equation can be solved using one of the following approaches:

(1) Delta-depletion approximation
(2) Exact analytical model
(3) Using numerical solution techniques

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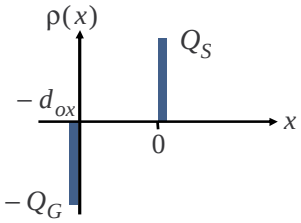
A. Delta-Depletion Approximation

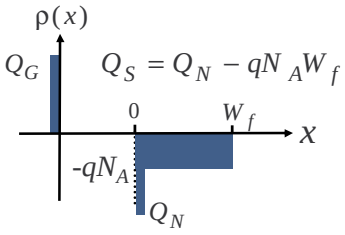
Accumulation:



- Accumulation charge is replaced with a delta-charge positioned right at the semiconductor interface.
- The electric field and the electro-static potential are:

$$F(x) = \varphi(x) = 0 \quad \text{for} \quad x > 0$$

Inversion:



- The charge associated with the minority carriers resides in an extremely narrow region at the SC/oxide interface.
- To first order we can assume that:

$$\varphi_s = 2\varphi_F \quad \text{for} \quad V_G > V_{th}$$

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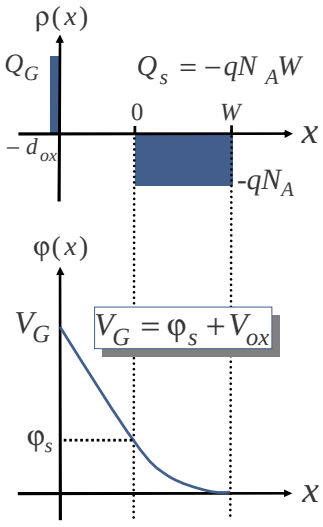
Depletion



- The charge density is given by:

$$\rho(x) = -qN_A$$

- The boundary conditions for the 1D Poisson equation are:

$$\varphi(W) = F(W) = 0, \quad \varphi(0) = \varphi_s$$

- Final expressions for the electric field, electrostatic potential and the width of the depletion region:

$$F(x) = \frac{qN_A}{k_s \varepsilon_0}(W - x)$$

$$\varphi(x) = \frac{qN_A}{2k_s \varepsilon_0}(W - x)^2$$

$$W = \sqrt{\frac{2k_s \varepsilon_0 \varphi_s}{qN_A}}$$

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Depletion, Cont'd

- The surface potential is an internal parameter. We therefore need to relate φ_s to the gate voltage V_G using:

$$V_G = V_{ox} + \varphi_s = F_{ox} d_{ox} + \varphi_s$$

where:

$$F_{ox} = \frac{k_s}{k_{ox}} F_s = \frac{k_s}{k_{ox}} \frac{qN_A W}{k_s \varepsilon_0} = \frac{qN_A W}{k_{ox} \varepsilon_0}$$

- Final expression for the V_G-φ_s relationship:

$$V_G = \varphi_s + \frac{1}{C_{ox}} \sqrt{2qN_A k_s \varepsilon_0 \varphi_s}, \quad \text{where} \quad C_{ox} = \frac{k_{ox} \varepsilon_0}{d_{ox}}$$

- Threshold voltage definition:

$$V_{th} = V_G \quad \text{for which} \quad \varphi_s = 2\varphi_F$$

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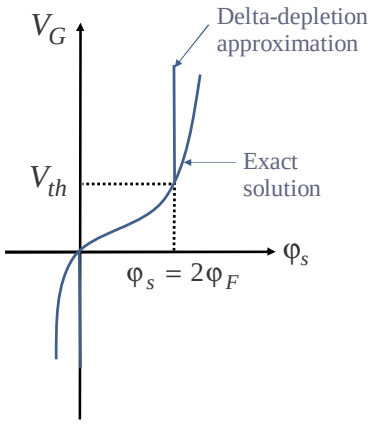
Depletion, Cont'd

- Graphical representation of the V_G-φ_s relationship:



- Surface potential varies rapidly with V_G when the device is **depletion biased**. Gate voltage is divided proportionally between the semiconductor and the oxide.
- When the semiconductor is **accumulated** or **inverted**, it takes large V_G to produce small change in φ_s. Changes in the applied bias are almost all dropped across the oxide.

B. Exact Analytical Model

- To solve for the electrostatic potential and the electric field profile under arbitrary bias conditions, one needs to go beyond the delta-depletion approximation and use the exact expression for the charge density $\rho(x)$ in the 1D Poisson equation:

$$\rho(x) = q(p - n + N_D - N_A)$$
$$= q\left(p_{po}e^{-\varphi/V_T} - n_{po}e^{\varphi/V_T} + N_D - N_A\right)$$

- Analytical tricks that we need to use to get to the answer:

(1) $\dfrac{d^2\varphi}{dx^2} = \dfrac{d}{dx}\left(\dfrac{d\varphi}{dx}\right) = \dfrac{d}{d\varphi}\left(\dfrac{d\varphi}{dx}\right)\dfrac{d\varphi}{dx} = \dfrac{udu}{d\varphi}, \quad u = \dfrac{d\varphi}{dx} = -F(x)$

(2) $\rho(x) = 0$ in the semiconductor bulk, where φ=0.

Exact Analytical Model, Cont'd

- Integrating the 1D Poisson equation from the bulk up to some point at a distance x from the SC/oxide interface (at which point the potential is φ) we get:

$$F^2(\varphi) = \frac{2qp_{po}V_T}{k_s\varepsilon_0}\underbrace{\left[\left(e^{-\varphi/V_T} + \frac{\varphi}{V_T} - 1\right) + \frac{n_{po}}{p_{po}}\left(e^{\varphi/V_T} - \frac{\varphi}{V_T} - 1\right)\right]}_{f^2(\varphi)}$$

- Now, introducing the extrinsic *Debye* length L_D, we can write:

$$L_D = \sqrt{\frac{k_s\varepsilon_0 V_T}{qp_{po}}} \rightarrow F(\varphi) = \pm\frac{\sqrt{2}V_T}{L_D}f(\varphi)$$

(+) sign is for positive φ
(-) sign is for negative φ

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Exact Analytical Model, Cont'd

- At the SC/oxide interface we have $\varphi=\varphi_s$, which leads to the following results for:

  (a) electric field: $F_s = F(\varphi_s) = \pm\sqrt{2}V_T\, f(\varphi_s)/L_D$

  (b) total sheet-charge density:

$$Q_s = -k_s\varepsilon_0 F_s$$
$$= \mp\frac{\sqrt{2}k_s\varepsilon_0 V_T}{L_D}\left[\left(e^{-\varphi_s/V_T}+\frac{\varphi_s}{V_T}-1\right)+\frac{n_{po}}{p_{po}}\left(e^{\varphi_s/V_T}-\frac{\varphi_s}{V_T}-1\right)\right]$$

  - flat-band condition: $\varphi_s = 0 \rightarrow Q_s = 0$
  - depletion regime: $0 < \varphi_s < 2\varphi_F \rightarrow Q_s < 0$
  - inversion regime: $\varphi_s > 2\varphi_F \rightarrow Q_s \propto -\exp(\varphi_s/2V_T)$
  - accumulation regime: $\varphi_s < 0 \rightarrow Q_s \propto \exp(-\varphi_s/2V_T)$

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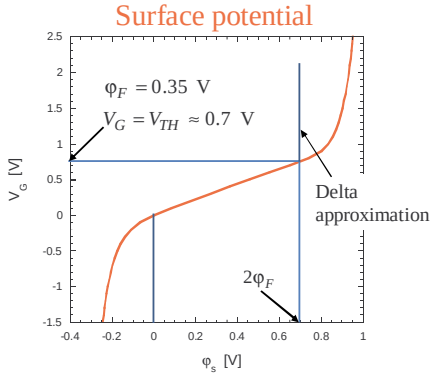
Exact Analytical Model, Cont'd

- The corresponding gate voltage equals to:

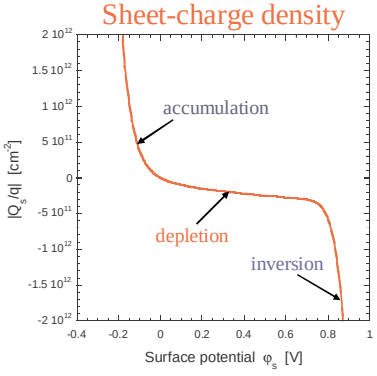
$$V_G = \varphi_s + V_{ox} = \varphi_s + \frac{k_s}{k_{ox}}F_s d_{ox}$$

- Simulation results for N_A=10^{16} cm^{-3} and d_{ox}=4 nm:

Surface potential



Sheet-charge density



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C. SCHRED: Self-Consistent Schrodinger-Poisson Solver

- SCHRED location:

  http://www.nanohub.org

- Existing SCHRED Features:
  - ➔ Classical and quantum-mechanical charge description

    Fermi-Dirac and Maxwell-Boltzmann Statistics (for classical)
    Fermi-Dirac for quantum-mechanical calculation
  - ➔ Multiple-valley conduction and valence bands
  - ➔ Metal and poly-silicon gates: SG and DG structures
  - ➔ Partial ionization of the impurity atoms
  - ➔ Exchange and correlation corrections to the ground state energy of the system

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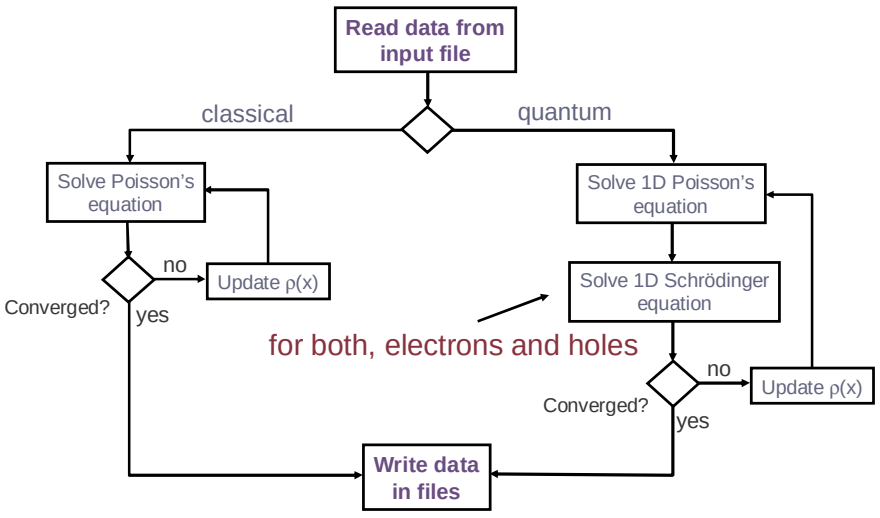
SCHRED Flow-Chart



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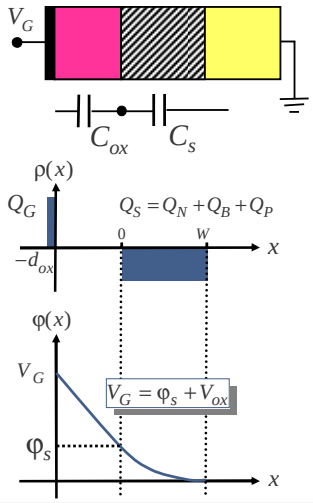
3. Ideal MOS Capacitor Capacitance

- The capacitance per unit area of an MOS capacitor is calculated using:

$$C_{tot} = \frac{dQ_G}{dV_G} = -\frac{dQ_s}{d(V_{ox}+\varphi_s)} = \frac{1}{-\frac{dV_{ox}}{dQ_s} - \frac{d\varphi_s}{dQ_s}}$$

$$= \frac{1}{1/C_{ox}+1/C_s} = \frac{C_{ox}}{1+C_{ox}/C_s}$$



where:

- C_{ox} is the oxide capacitance
- C_s is the SC capacitance

Ideal MOS Capacitor Capacitance, Cont'd

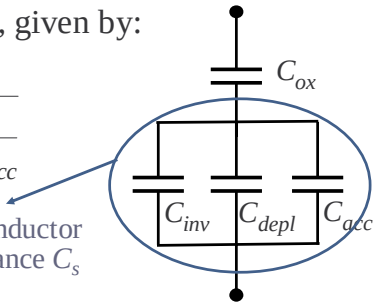
- In general, the charge in the semiconductor is represented as a sum of the inversion layer charge density Q_N, depletion layer charge density Q_B and the accumulation layer charge density Q_P, which gives:

$$C_s = -\frac{dQ_s}{d\varphi_s} = -\frac{dQ_N}{d\varphi_s} - \frac{dQ_B}{d\varphi_s} - \frac{dQ_P}{d\varphi_s} = C_{inv} + C_{depl} + C_{acc}$$

- The total gate capacitance is, thus, given by:

$$C_{tot} = \frac{C_{ox}}{1+C_{ox}/C_s} = \frac{C_{ox}}{1+\frac{C_{ox}}{C_{inv}+C_{depl}+C_{acc}}}$$

$$C_{ox} = \frac{k_{ox}\varepsilon_0}{d_{ox}}$$



Ideal MOS Capacitor Capacitance - Accumulation

- Using the analytical model expression for the semiconductor charge per unit area Q_s, we get:

$$C_s = -\frac{dQ_s}{d\varphi_s} = Cso\frac{\left|1 - e^{-\varphi_s/V_T} + \frac{n_{po}}{p_{po}}\left(e^{\varphi_s/V_T} - 1\right)\right|}{\sqrt{2}f(\varphi_s)}$$

$$f(\varphi_s) = \left[e^{-\varphi_s/V_T} + \frac{\varphi_s}{V_T} - 1 + \frac{n_{po}}{p_{po}}\left(e^{\varphi_s/V_T} - \frac{\varphi_s}{V_T} - 1\right)\right]^{1/2}$$

$$C_{so} = \frac{k_s\varepsilon_0}{L_D} \rightarrow \text{Flat-band capacitance}$$

(A) Accumulation regime:

$$\left.\begin{array}{l}\varphi_s < 0 \rightarrow f(\varphi_s) \propto \exp\left(-\varphi_s / 2V_T\right) \\ dQ_N = 0, \quad dQ_B = 0\end{array}\right\} \rightarrow C_{tot} \approx C_{ox}$$

The total gate capacitance is approximately equal to the oxide capacitance.

Depletion Regime

(B) Depletion regime:

- In depletion regime, the inversion charge is negligible when compared to the depletion charge. Hence:

$$\left.\begin{array}{l}0 < \varphi_s < 2\varphi_F \rightarrow f(\varphi_s) \propto \sqrt{\varphi_s / V_T} \\ dQ_N = 0, \quad dQ_P = 0\end{array}\right\} \rightarrow C_s = \frac{Cso}{\sqrt{2\varphi_s / V_T}} = \sqrt{\frac{k_s\varepsilon_0 qN_A}{2\varphi_s}}$$

- The total capacitance is, thus, given by:

$$C_{tot} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_s}} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{depl}}} = \frac{k_{ox}\varepsilon_0}{d_{ox} + k_{ox}\varepsilon_0\sqrt{\frac{2\varphi_s}{k_s\varepsilon_0 qN_A}}}$$

- Important remarks:
  - If N_A increases, then C_{tot} increases.
  - If d_{ox} increases, C_{tot} decreases.

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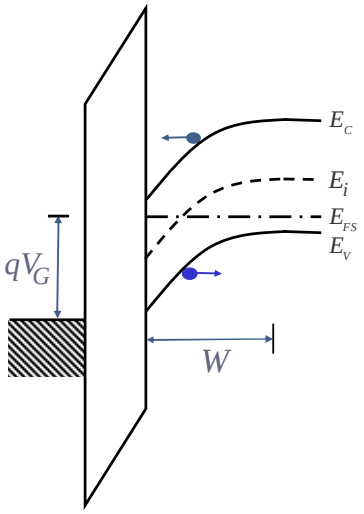
Inversion Regime

(C) Inversion regime:

- Most of the charge induced at the SC-oxide interface comes from the electron-hole pair generation (via recombination-generation centers).
- The build-up of minority carriers proceeds at a rate limited by the process of generation of electron-hole pairs.
- Hence, depending upon the frequency of the applied signal and the sweep-rate of the gate voltage, one can measure:
  - low-frequency (LF) ***CV***-curves
  - high-frequency (HF) ***CV***-curves
  - deep-depletion (DD) ***CV***-curves



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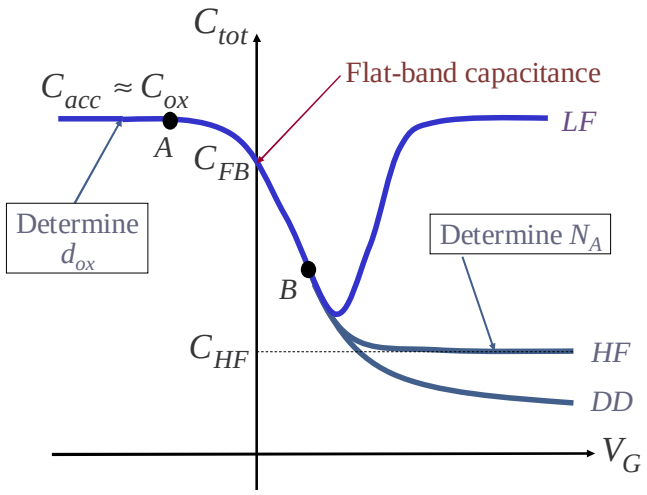
Capacitance Under Different Conditions

Graphical illustration of the three different cases:



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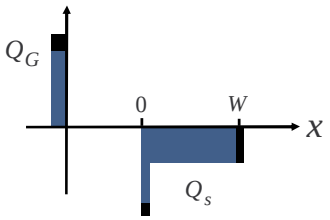
Low-Frequency CV-curve

- *AC*-frequency low and sweep-rate low to allow for the generation of the inversion layer electrons and their response to the applied *AC* signal.



- Inversion layer and total gate capacitance:

$$\varphi_s > 2\varphi_F \rightarrow \left.\begin{array}{l} f(\varphi_s) \propto \exp(\varphi_s / 2V_T) \\ dQ_P = 0 \end{array}\right\} \rightarrow C_s \approx C_{inv} \approx C_{so}\sqrt{\frac{n_{po}}{2p_{po}}}e^{\varphi_s/2V_T}$$

$$C_{tot} = \frac{C_{ox}}{1+C_{ox}/C_s} = \frac{C_{ox}}{1+C_{ox}/C_{inv}} \approx C_{ox}$$

The total gate capacitance is approximately equal to the oxide capacitance.

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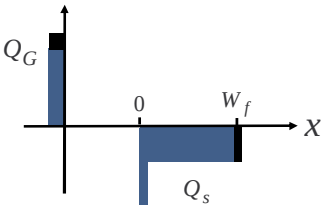
High-Frequency CV-Curve

- *AC*-frequency high, which prevents the response of the minority carriers. The sweep-rate is low, thus allowing for the generation of the inversion layer electrons.



- Depletion layer and total gate capacitance:

$$\varphi_s \approx 2\varphi_F \rightarrow \left.\begin{array}{l} f(\varphi_s) = \sqrt{2\varphi_F / V_T} \\ dQ_N = 0, \quad dQ_P = 0 \end{array}\right\} \rightarrow C_s \approx C_{depl} \approx \sqrt{\frac{k_s \varepsilon_0 q N_A}{2(2\varphi_F)}}$$

$$C_{tot} = \frac{C_{ox}}{1+C_{ox}/C_{depl}} = \frac{C_{ox}}{1+C_{ox}\sqrt{\frac{2(2\varphi_F)}{k_s\varepsilon_0 q N_A}}} \approx const$$

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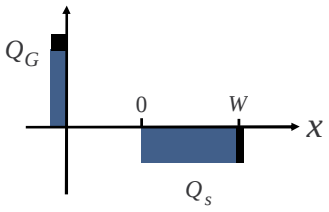
Deep-Depletion CV-Curve

- *AC*-frequency high, which prevents the response of the minority carriers. The sweep-rate is also high, thus preventing the generation of the inversion layer electrons.



- Depletion layer and total gate capacitance:

$$\left.\begin{array}{l} f(\varphi_s) = \sqrt{\varphi_s / V_T} \\ dQ_N = 0, \;\; dQ_P = 0 \end{array}\right\} \rightarrow C_s \approx C_{depl} \approx \sqrt{\frac{k_s \varepsilon_0 q N_A}{2\varphi_s}}$$

$$C_{tot} = \frac{C_{ox}}{1 + \frac{C_{ox}}{C_{depl}}} = \frac{C_{ox}}{1 + C_{ox}\sqrt{\frac{2\varphi_s}{k_s \varepsilon_0 q N_A}}}$$

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What is Low Frequency?

- The SCR generation current density equals to:

$$J_{SCR} = q n_i W / \tau_g$$

- While J_{SCR} flows in the semiconductor, the current flowing through the oxide is:

$$J_D = C_{ox} dV / dt$$

- For the inversion charge to be able to respond, we must have that the SCR current must be able to supply the required displacement current, *i.e.*

$$C_{ox} dV / dt \le q n_i W / \tau_g \rightarrow dV / dt \le \frac{q n_i W}{C_{ox} \tau_g}$$

Example: d_{ox}=100 nm, W=1 μm, C_{ox}=3.45×10^{-8} F/cm^2 :

τ_g=10 μs, $dV/dt \le 0.65$ V/s, f_{eff}=45 Hz (not a severe constraint)

τ_g=1 ms, $dV/dt \le 6.5$ mV/s, f_{eff}=0.4 Hz (severe constraint)

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4. Deviations from the Ideal Model

There are several factors that lead to deviation of the measured *CV*-curves from what the ideal model predictions are:

- Work-function difference
- Oxide charges (interface-trap, fixed-oxide, oxide-trap and mobile oxide charges)
- Depletion of the poly-silicon gates
- Quantum-mechanical space-quantization effects

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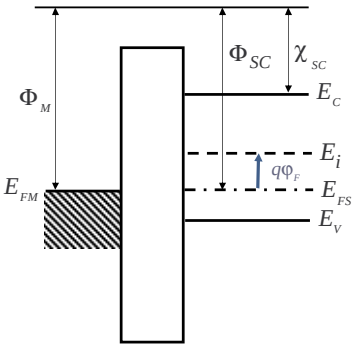
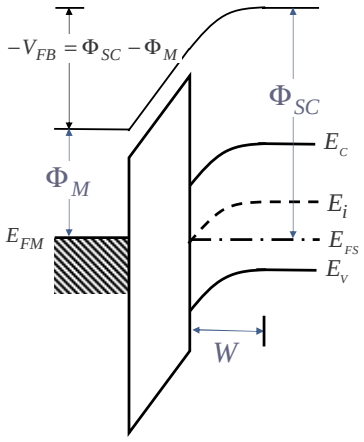
A. Workfunction Difference

Ideal MOS capacitor with a *p*-type semiconductor



$$\Phi_M = \chi_{sc} + \frac{E_g}{2} + q\varphi_F$$

Real MOS capacitor with a *p*-type semiconductor



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Workfunction Difference, Cont'd

- The flat-band voltage V_{FB} equals the required gate voltage to achieve flat-band conditions.
- The workfunction difference modifies the relationship between the surface potential and the applied bias. This gives rise to threshold voltage shift between the ideal and real *CV*-curves:

$$\Delta V_G = V_G - V_G' = \frac{1}{q}\Phi_{MS} = \frac{1}{q}(\Phi_M - \Phi_{SC})$$

Voltage applied to real MOS capacitor

Voltage applied to ideal MOS capacitor

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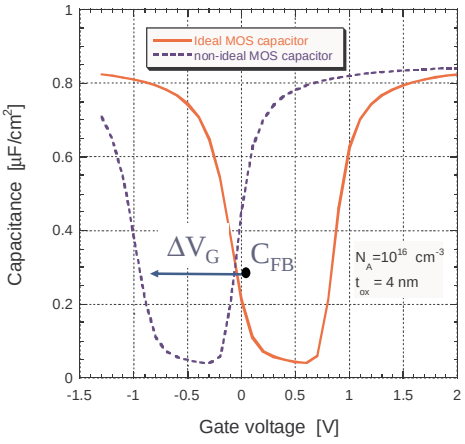
Simulation Example

- Influence on the *LF CV*-curves:



- Same effect is also observed on the *HF* and the *DD CV*-curves.

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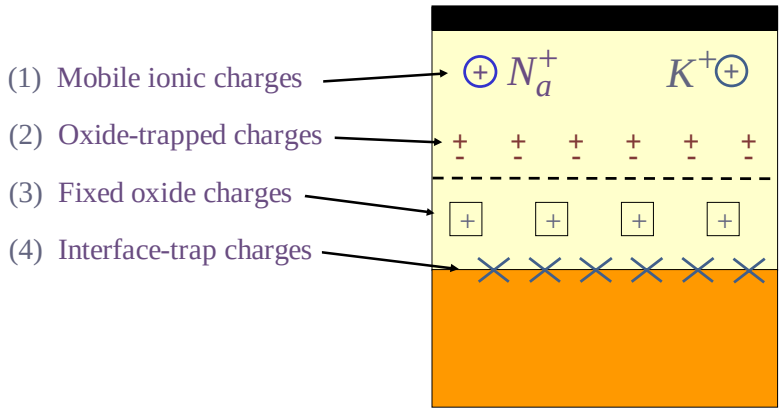
B. Oxide Charges

- The charges that exist in a realistic MOS structure can be classified into four different categories:



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Oxide Charges, Cont'd

- Mobile oxide charges: Due to ionic impurities such as Na, K, etc.
- Oxide-trapped charge: May be positive or negative and is due to holes or electrons trapped in the bulk of the oxide.
- Fixed oxide charges: Due to structural defects (ionized silicon) in the oxide layer.
- Interface-trapped charges: Positive or negative charges due to:
  - structural, oxidation induced defects
  - metal impurities
  - other defects due to bond-breaking processes

Unlike other oxide charges, interface-trapped charge is in electrical communication with the underlying silicon and can be charged and discharged.

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Oxide Charges, Cont'd

- The expression for the voltage drop across the oxide layer V_{ox} in the presence of a non-zero charge distribution $\rho(x)$ is found from the solution of the 1D Poisson equation, using the boundary conditions: $\varphi_{ox}(0)=0$ and $\varphi_{ox}(d_{ox})=V_{ox}$.
- The final result of this calculation is given below:

$$V_{ox} = d_{ox}F_{ox}(d_{ox}) - \gamma\frac{Q_{ox}}{C_{ox}}, \quad \gamma = \frac{1}{d_{ox}}\frac{\int_0^{d_{ox}} x\rho_{ox}(x)dx}{\int_0^{d_{ox}} \rho_{ox}(x)dx}$$

- Special cases:
  1. uniform charge distribution: $\gamma=1/2$
  2. Charges at the SC/oxide interface: $\gamma=1$
  3. Charges at the metal/oxide interface: $\gamma=0$

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Oxide Charges, Cont'd

- The threshold voltage shift due to workfunction difference and charges in the oxide is given by:

Oxide charges

Work function difference

$$\Delta V_G = V_G - V_G' = -\gamma\frac{Q_{ox}}{C_{ox}} + \frac{1}{q}\Phi_{MS} = V_{FB}$$

Flat-band voltage

Voltage applied to real MOS capacitor with oxide charges

Voltage applied to ideal MOS capacitor

- Important note: All the charges (mobile ion charges, fixed oxide charges, oxide trapped charges) except the interface-trap charges lead to rigid shift of the CV curve.

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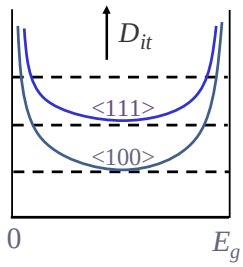
Interface-Trapped Charges

- More information on interface-trapped charges:
  - Most of the interface-trapped charges can be neutralized by low-temperature hydrogen annealing.
  - The interface trap density is given by:

$$D_{it} = \frac{1}{q}\frac{dQ_{it}}{dE}\left(\frac{\#\text{ of charges}}{cm^2 eV}\right)$$



  - Interface trap charges can be:
    - acceptor-like (above the intrinsic level)
    - donor-like (below the intrinsic level)

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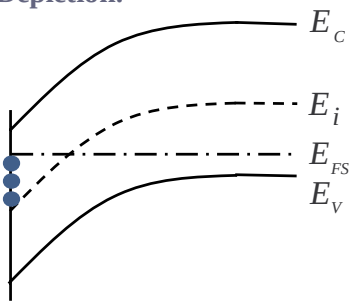
Interface-Trapped Charges, Cont'd

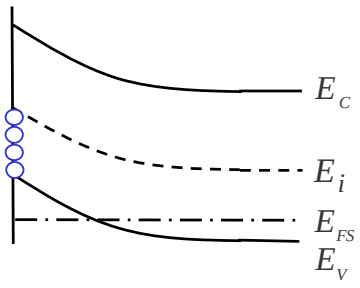
- Use simplified model that all of the states below the Fermi level are full and all of the states above the Fermi level are empty.

Depletion:



The excess negative charges lead to positive shift.

Accumulation:



The excess positive charges lead to negative shift.

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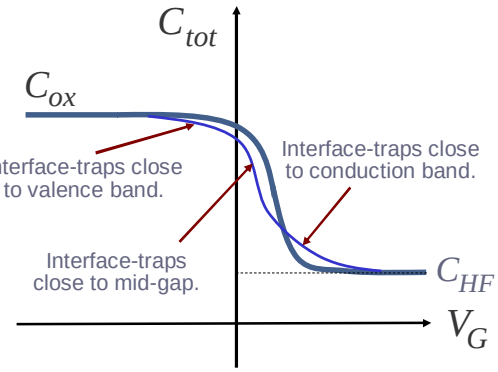
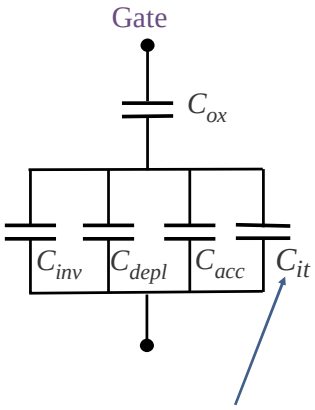
Interface-Trapped Charges, Cont'd

- Modification of the *HF-CV* curve due to interface-trapped charges.





Contribution from the charging and discharging of the interface traps.

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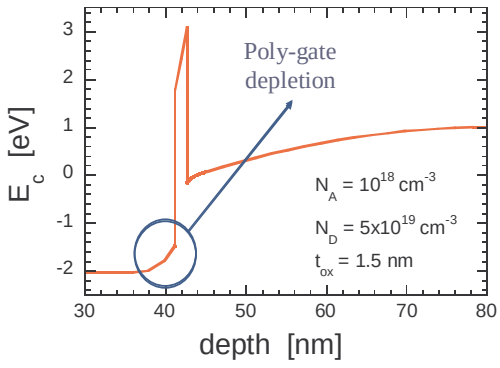
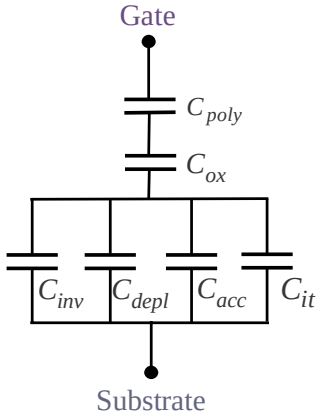
C. Depletion of the Poly-Silicon Gates

In real MOS capacitors, the gate is usually made of heavily-doped poly-silicon. Even though the doping of the poly-silicon gate is large, there is always some finite depletion region, which gives rise to poly-gate capacitance C_{poly} that degrades C_{tot}.





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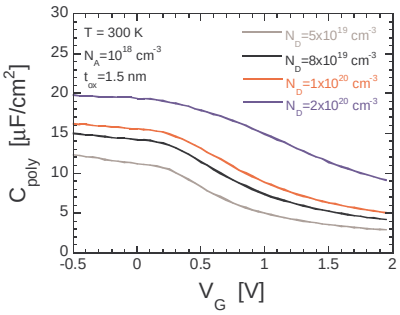
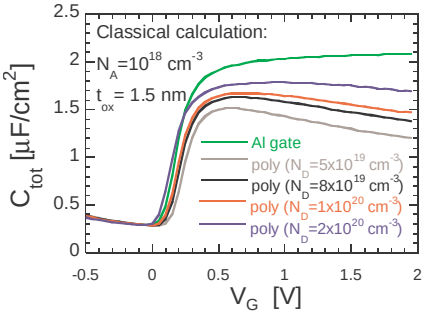
SCHRED Simulation Results

- Simulation results obtained with SCHRED. They clearly show the role of poly-gate depletion on C_{tot}.





Important remark:

- The poly-gate depletion introduces gate-voltage dependence on the total gate capacitance in strong inversion conditions for MOS capacitors on *p*-type substrates.

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Example 1: MOS Capacitor-Semiclassical Model (Padre MOS Capacitor)

Problem Statement:

Consider a simple MOS capacitor. The gate is made of aluminum, the thickness of the SiO_2 layer is t_{ox}=4 nm and the doping of the p-type substrate is $N_A=10^{18}$ cm^{-3}. For this device structure plot:

At equilibrium

(a) the electrostatic potential,
(b) the total charge density,
(c) the electric field profile.

Under applied gate bias of 2V

(a) the inversion electron density vs. position

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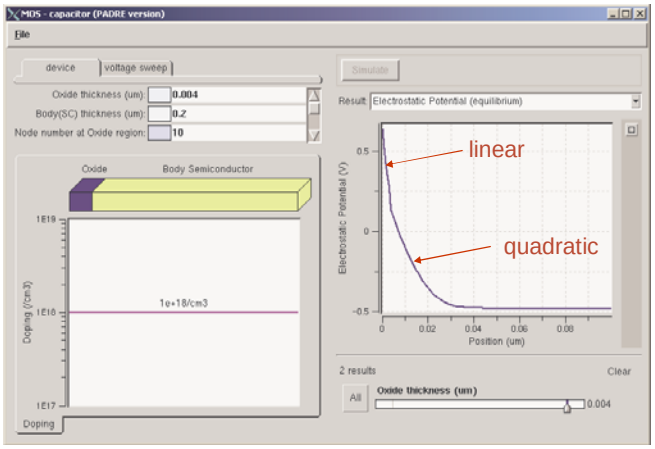
Electrostatic Potential



Since there are no charges in the oxide, the variation of the electrostatic potential in the oxide region is linear. In the semiconductor, due to the presence of the depletion region, we have quadratic variation of the potential vs. depth.

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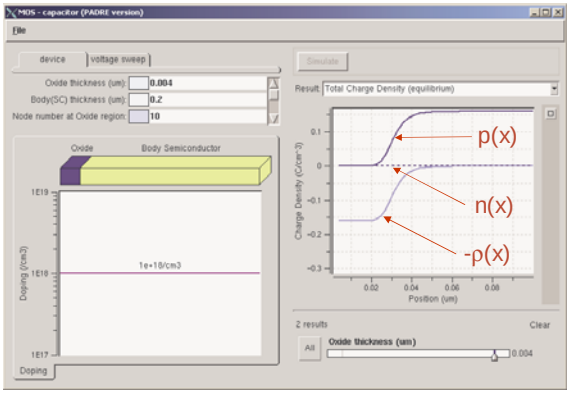
Electron Density



The total charge density in this particular case equals the $N_A(x) + n(x) – p(x)$. The electron density is negligible, which means that the inversion layer has not formed yet. Therefore the net charge density is $N_A(x) - p(x)$ and depicts the exten-sion of the depletion region in the semiconductor.

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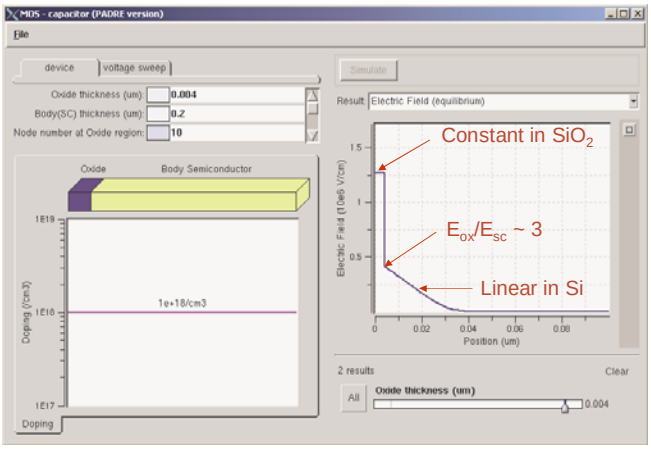
Electric Field Profile



The electric field is constant in the oxide, varies linearly in the semiconductor since the doping is constant and the ratio of the electric fields in the oxide and in the semiconductor at the sc/oxide interface equals the ratio of sc/oxide dielectric constants.

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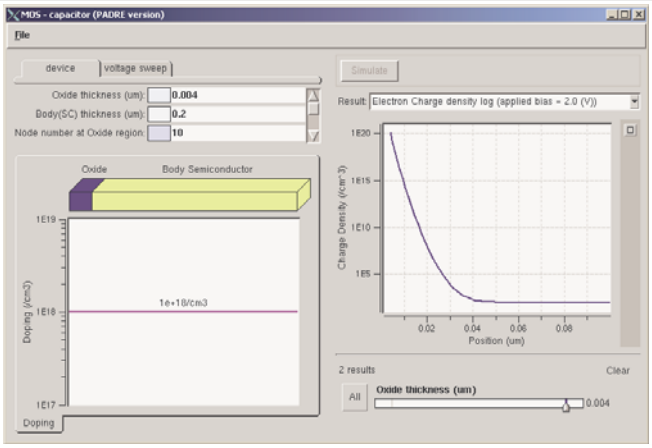
Electron Density Under Bias



For V_G=2V, the inversion layer has formed. Since the potential is peaked at the sc/oxide interface, the electron density peaks at the interface and then decays exponentially into the bulk semiconductor region. This is what the classical picture predicts.

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Example 2: Workfunction Difference, Doping Dependence (PADRE simulation)

Problem Statement:

Consider a MOS capacitor structure found in conventional MOSFET devices. The thickness of the oxide region equals 4 nm and the substrate is p-type with doping N_A.

(a) Assume that $N_A=10^{17}$ cm^{-3}. Plot the conduction band profile under equilibrium conditions assuming aluminum gate, n+-polysilicon and p+-polysilicon gate.
(b) Vary the gate voltage from -2 to 2 V and calculate the high-frequency CV curves using f=1MHz. How does the change in the type of the gate electrode (aluminum vs. n+-polysilicon vs. p+-polysilicon) reflects on the HF CV-curves.
(c) Assume aluminum gate and plot the HF CV-curves for f=1MHz. How does the change in substrate doping reflects itself on the HF CV-curves. Support your reasoning with a physical model. Assume that $N_A=10^{16}$, 10^{17} and 10^{18} cm^{-3}.

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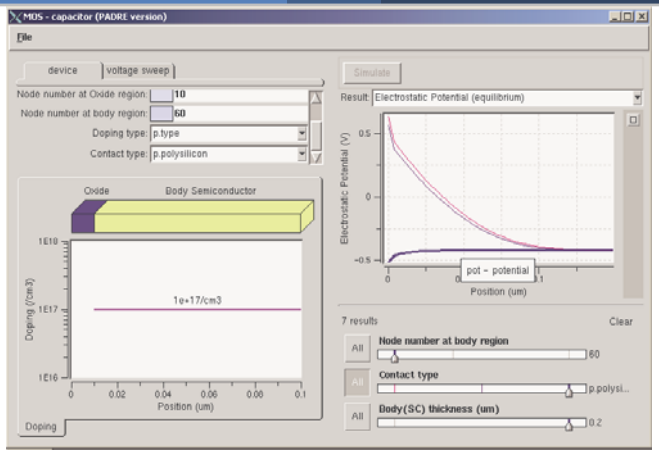
Electrostatic Potential



The aluminum and the n+-polysilicon gate make the MOS capacitor to be in the depletion/inversion mode. The very large value of the workfunction of the p+-polysilicon gate completely switches the picture and reverts it to accumulation mode.

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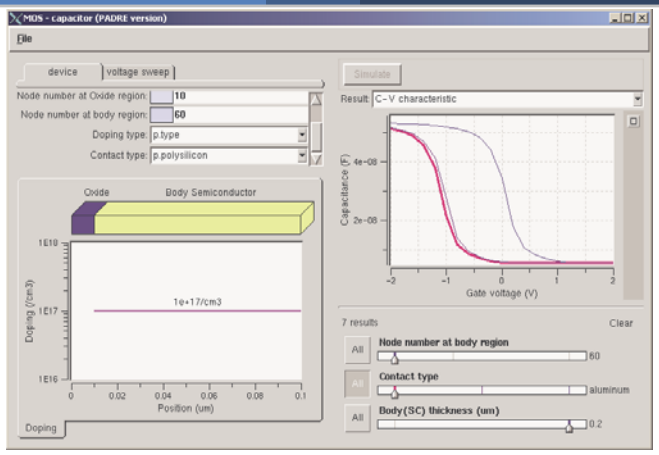
CV-Curve – Different Electrode



The change in the type of the gate electrode affects the metal-semiconductor workfunction difference and leads to rigid shift of the HF CV-curves. There is no distortion of the curves that can be produced, for example, by interface traps.

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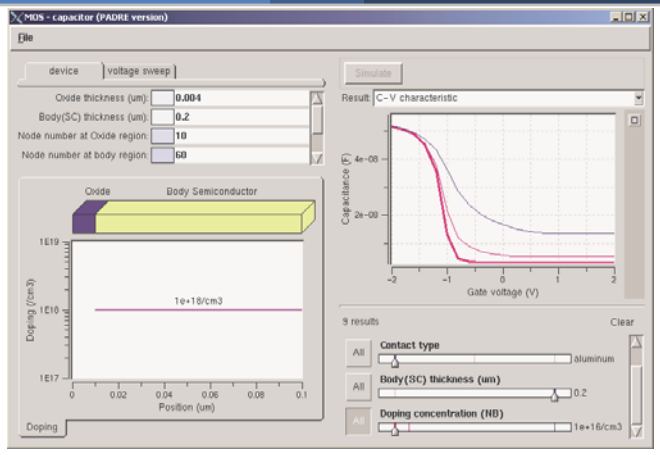
CV-Curve – Different Doping



The total gate capacitance under depletion conditions is a serial combination of the oxide and of the depletion layer capacitance. Since the thickness of the depletion layer varies as $N_A^{-1/2}$, with increasing N_A the depletion capacitance increases.