

Computational Electronics

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Development of the Transistor Era

The seeds of development that were planted during World War Two and nourished by urgent military requirements started to flower after the war and produced technological marvels that kept the United States in the forefront of science. Two of the major events include the development of the digital computer and the germanium point–contact transistor. The trillion–dollar economy of many large countries and the landing of men on the moon would not have been possible without these two essential inventions.

The first digital, computer evolved from theories put forth by John Mauchly and John Presper Eckert in a proposal to the U.S. Army in 1943, when a machine that could rapidly calculate ballistic trajectories for large guns was desperately needed. However, it wasn't until 1946 at the University of Pennsylvania that Eckert and Madchly had a working machine — the ENIAC [1]. But programming the ENIAC required large wiring panels and was not very flexible; a simple program change could take hours. Later that year John von Neumann [2], a mathematician who helped develop the atom bomb during World War Two, proposed an electronic computer, which he would eventually help develop, with a memory that would permit stored programs and other internally stored information. The original ENIAC computer did over 5000 arithmetic calculations per second, weighed over 30 tons, contained more than 18,000 vacuum tubes and consumed 130 kilowatts. Large quantities of tubes, such as ENIAC used, were incorporated into many telecommunications networks being built at that time. But tubes, when grouped in large numbers, are power hungry. Many companies started to look for a low–power alternative.

Finally, in late 1947, the Bell Laboratories research team of John Bardeen, Walter Brattain and William Shockley succeeded [3]. They developed what was later named the germanium point–contact transistor, considered the beginning of the modern electronics industry. Actually, the team only "rediscovered" the transistor concept, for back in 1929 an engineer named Julius Lillienfeld [4] patented what today would be called a metal–oxide field–effect transistor. His discovery faded away in a short time since the materials required to build the device just couldn't be made pure enough, and worse, the money needed for further development wasn't available because the U.S. was just entering the Great Depression and venture capital for research projects just was not around. As a result, the semiconductor age started in the late 1940s.

The point-contact transistor developed by Bell Laboratories in late 1947 and announced to the world in 1948 was a delicate device and very hard to produce. The hardest problem was the manufacture of the semiconductor material itself. Germanium was readily available, but it had to be purer than available processing methods could produce in quantity. Work was started on refining processes by Jack Scaff and William Pfann at Bell Laboratories. Research at General Electric, RCA, and at Bell Labs paid off in an alloying technique that produced commercially feasible transistors. The Czochralski technique of growing large quantities of single crystal germanium was perfected, an absolute necessity if transistors were to be produced in high volume and at low cost. Along with the promises that zone refining and crystal growing were soon to keep, improved semiconductor devices were starting to appear in the laboratory. The junction transistor made its appearance as a result of work by Morgan Sparks at Bell Laboratories. It was free of the mechanical problems of the point-contact transistor and was much more rugged. The junction was constructed by heat alloying two "blobs" of indium (one on each side) onto a germanium crystal. The alloying process produced the collector and emitter regions on the crystal; the area in which no alloying occurred served as the base. The alloy transistor offered the possibility of ultra-low-power operation because just one or two microwatts were needed to power the transistor. Hundreds or even thousands of these transistors could operate from the same power needed to heat the filament of a single vacuum tube. With transistors on the verge of replacing vacuum tubes, many other advances were making the change a necessity rather than a nicety. The power drain of complex digital and telecommunications systems had to be cut.

Until 1954 many companies had been striving to perfect the germanium transistor. In the process, the team of Gordon Teal and Ernest Buehler at Bell Labs perfected a method of growing single-crystal silicon. This development, combined with the groundwork done by William Pfann in creating the material-purification process known as zone refining, laid the foundation for today's multibillion-dollar semiconductor industry. Texas Instruments, building on the work of Calvin Fuller of Bell Labs, introduced the first silicon transistors in 1954. Fuller developed the process of diffusing impurities into the surface of a silicon wafer, paving the way for the development of the integrated circuit, which was announced a few years later by TI. The first consumer products that contained transistors appeared on the market between 1952 and 1954. A transistorized hearing aid and a four-transistor radio were two of the first. William Shockley

extended his original two-junction transistor with three and four-junction devices. His theories were put to use by Gerald Pearson at Bell Laboratories in 1954, in the development of thyristors.

The first years of the transistor era had not particularly affected tube manufacturers. Transistors were very expensive and at high frequencies they were still quite limited in power-handling capability. In 1954 the highest rated transistor could handle about seven watts at a frequency of 5000 hertz. To boost the capabilities of the transistor, N. H. Fletcher, an engineer at Transistor Products, reshaped the emitter and base patterns into finger-like interwoven structures in a process that soon became known as interdigitation. This pattern is still used in almost every high-frequency power transistor made. After Fletcher's developments transistors started to threaten some tube applications and the vacuum-tube industry began to fight back. Sylvania, using ceramic insulators instead of mica, developed the stacked vacuum tube to produce greater ruggedness than had previously been available. It still had a filament, though, and as transistors improved in performance, the stacked tube fell by the wayside.

One of the earliest commercial products to evolve from the development of single-crystal silicon was the Zener diode, originally manufactured by National Fabricated Products. The Zener diode was the first solid-state voltage-regulating element. Texas Instruments and Fairchild Corp. announced their development of integrated circuits in late 1958. The circuits were crude — they contained several transistors, a few resistors and some capacitors — compared with the ten thousand or so transistors now possible on a single silicon chip. General Electric and Crystalonics introduced commercial field-effect transistors in 1958 as an outgrowth of theories put forth by Shockley in the early 1950s. Developments announced earlier by Texas Instruments and Fairchild had marked the beginning of the era of the integrated circuit. Within a few years the complexity of the circuits had grown so that entire systems could be economically placed onto a single quarter-inch-square silicon chip. The space age was also beginning — with orbital satellites and attempts to get close-up pictures of the moon. When we looked at those attempts then, we marveled at them. And yet, on July 4, 1976 we will land an automated probe on the surface of the planet Mars.

Computational Electronics

As semiconductor feature sizes shrink into the nanometer scale regime, even conventional device behavior becomes increasingly complicated as new physical phenomena at short dimensions occur, and limitations in material properties are reached [5]. In addition to the problems related to the understanding of actual operation of ultra-small devices, the reduced feature sizes require more complicated and time-consuming manufacturing processes. This fact signifies that a pure trial-and-error approach to device optimization will become impossible since it is both too time consuming and too expensive. Since computers are considerably cheaper resources, simulation is becoming an indispensable tool for the device engineer. Besides offering the possibility to test hypothetical devices which have not (or could not) yet been manufactured, simulation offers unique insight into device behavior by allowing the observation of phenomena that can not be measured on real devices. *Computational Electronics* [6,7] in this context refers to the physical simulation of semiconductor devices in terms of charge transport and the corresponding electrical behavior. It is related to, but usually separate from process simulation, which deals with various physical processes such as material growth, oxidation, impurity diffusion, etching, and metal deposition inherent in device fabrication [8] leading to integrated circuits. Device simulation can be thought of as one component of technology for computer-aided design (TCAD), which provides a basis for device modeling, which deals with compact behavioral models for devices and sub-circuits relevant for circuit simulation in commercial packages such as SPICE [9]. The relationship between various simulation design steps that have to be followed to achieve certain customer need is illustrated in **Figure 1**.

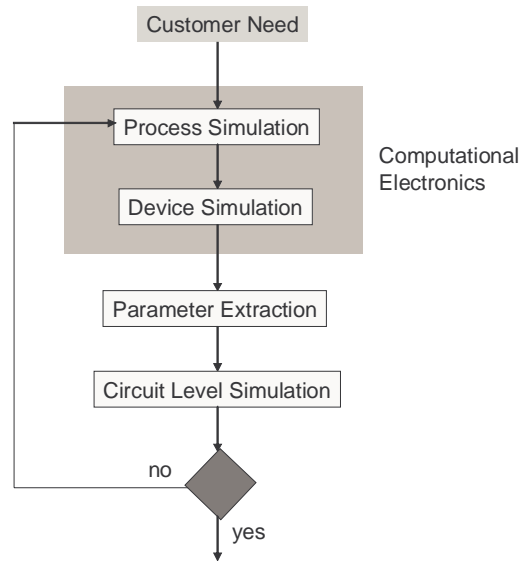


Figure 1 Design sequence to achieve desired customer need.

The goal of *Computational Electronics* is to provide simulation tools with the necessary level of sophistication to capture the essential physics while at the same time minimizing the computational burden so that results may be obtained within a reasonable time frame. Figure 2 illustrates the main components of semiconductor device simulation at any level. There are two main kernels, which must be solved self-consistently with one another, the transport equations governing charge flow, and the fields driving charge flow. Both are coupled strongly to one another, and hence must be solved simultaneously. The fields arise from external sources, as well as the charge and current densities which act as sources for the time varying electric and magnetic fields obtained from the solution of Maxwell's equations. Under appropriate conditions, only the quasi-static electric fields arising from the solution of Poisson's equation are necessary.

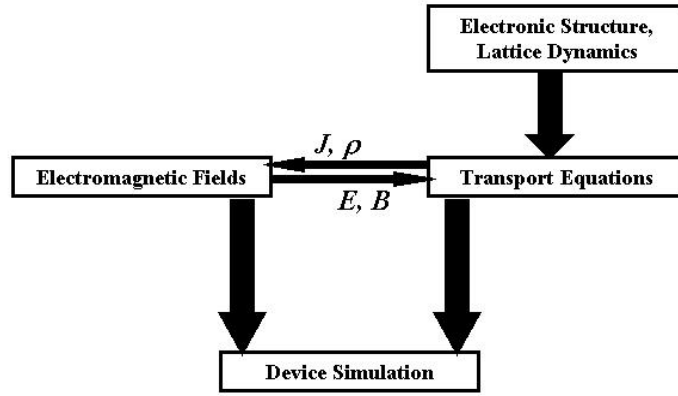


Figure 2. Schematic description of the device simulation sequence.

The fields, in turn, are driving forces for charge transport as illustrated in Figure 3 for the various levels of approximation within a hierarchical structure ranging from compact modeling at the top to an exact quantum mechanical description at the bottom. At the very beginnings of semiconductor technology, the electrical device characteristics could be estimated using simple analytical models (gradual channel approximation for MOSFETs) relying on the drift-diffusion (DD) formalism. Various approximations had to be made to obtain closed-form solutions, but the resulting models captured the basic features of the devices [10]. These approximations include simplified doping profiles and device geometries. With the ongoing refinements and improvements in technology, these approximations lost their basis and a more accurate description was required. This goal could be achieved by solving the DD equations numerically. Numerical simulation of carrier transport in semiconductor devices dates back to the famous work of Scharfetter and Gummel [11], who proposed a robust discretization of the DD equations which is still in use today.

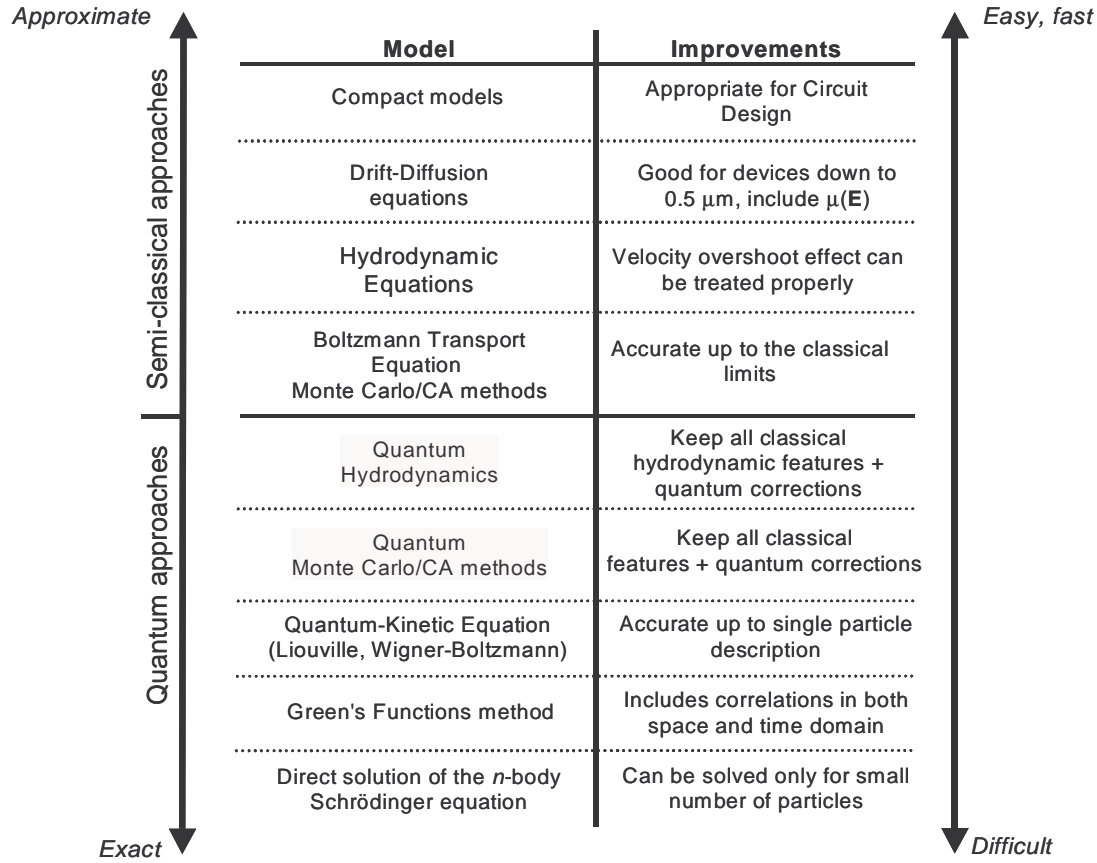


Figure 3. Illustration of the hierarchy of transport models.

However, as semiconductor devices were scaled into the submicrometer regime, the assumptions underlying the DD model lost their validity. Therefore, the transport models have been continuously refined and extended to more accurately capture transport phenomena occurring in these devices. The need for refinement and extension is primarily caused by the ongoing feature size reduction in state-of-the-art technology. As the supply voltages can not be scaled accordingly without jeopardizing the circuit performance, the electric field inside the devices has increased. A large electric field which rapidly changes over small length scales gives rise to non-local and hot-carrier effects which begin to dominate device performance. An accurate description of these phenomena is required and is becoming a primary concern for industrial applications.

To overcome some of the limitations of the DD model, extensions have been proposed which basically add an additional balance equation for the average carrier energy [12]. Furthermore, an additional driving term is added to the current expression which is proportional

to the gradient of the carrier temperature. However, a vast number of these models exist, and there is a considerable amount of confusion as to their relation to each other. It is now a common practice in industry to use standard hydrodynamic models in trying to understand the operation of as-fabricated devices, by adjusting any number of phenomenological parameters (e.g. mobility, impact ionization coefficient, etc.). However, such tools do not have predictive capability for ultra-small structures, for which it is necessary to relax some of the approximations in the Boltzmann transport equation [13]. Therefore, one needs to move downward to the quantum transport area in the hierarchical map of transport models shown in Figure 3 where, at the very bottom we have the Green's function approach [14,15,16]. The latter is the most exact, but at the same time the most difficult of all. In contrast to, for example, the Wigner function approach (which is Markovian in time), the Green's functions method allows one to consider simultaneously correlations in space and time, both of which are expected to be important in nano-scale devices. However, the difficulties in understanding the various terms in the resultant equations and the enormous computational burden needed for its actual implementation make the usefulness in understanding quantum effects in actual devices of limited values. For example, the only successful utilization of the Green's function approach commercially is the NEMO (Nano-Electronics MOdeling) simulator [17], which is effectively 1D and is primarily applicable to resonant tunneling diodes.

From the discussion above it follows that, contrary to the recent technological advances, the present state of the art in device simulation is currently lacking in the ability to treat these new challenges in scaling of device dimensions from conventional down to quantum scale devices. For silicon devices with active regions below 0.2 microns in diameter, macroscopic transport descriptions based on drift-diffusion models are clearly inadequate. As already noted, even standard hydrodynamic models do not usually provide a sufficiently accurate description since they neglect significant contributions from the tail of the phase space distribution function in the channel regions [18,19]. Within the requirement of self-consistently solving the coupled transport-field problem in this emerging domain of device physics, there are several computational challenges, which limit this ability. One is the necessity to solve both the transport and the Poisson's equations over the full 3D domain of the device (and beyond if one includes radiation effects). As a result, highly efficient algorithms targeted to high-end computational platforms (most likely in a multi-processor environment) are required to fully

solve even the appropriate field problems. The appropriate level of approximation necessary to capture the proper non-equilibrium transport physics relevant to a future device model is an even more challenging problem both computationally and from a fundamental physics framework.

In this course, we give an overview of the basic techniques used in the field of *Computational Electronics* related to device simulation. The multiple scale transport in doped semiconductors is summarized in Figure 4 in terms of the transport regimes, relative importance of the scattering mechanisms and possible applications.

	$L \ll l_{e-ph}$			$L \sim l_{e-ph}$	$L \gg l_{e-ph}$
	$L < \lambda$	$L < l_{e-e}$	$L \gg l_{e-e}$		
Transport Regime	Quantum	Ballistic	Fluid	Fluid	Diffusive
Scattering	Rare	Rare	e-e (Many), e-ph (Few)		Many
Model:					
	Quantum Hydrodynamic				
Schrodinger/Green's Functions					
Applications	Nanowires, Superlattices	Ballistic			
		Transistor	Current IC's	Current IC's	Older IC's

Figure 4. Relationship between various transport regimes and significant length-scales.

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