Dual-Gate JFET Modeling II: Source Pinchoff Voltage and Complete I_{ds} Modeling Formalism

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***Abstract*— This paper studies the phase diagram of source pinchoff of dual-gate JFETs and presents a source pinchoff modeling formalism that is smooth across the phase boundaries. Based on this, an I_{ds} model is derived, which is numerically robust for any value of top- and bottom-gate voltages. The method is applied to both the exact model for I_{ds} and an approximated form based on mid-point-potential linearization, and is verified by comparison with numerical simulation. Modeling of short-channel effects is included.**

***Index Terms*— JFETs, semiconductor device modeling, SPICE.**

I. Introduction

In [1], WE generalized the dual-gate JFET concept to include MOS as well as p-n junction gates and, for such devices, derived an I_{ds} model that is valid when the source[1] is not pinched off. In this paper, we extend our model to cover the case of source pinchoff, which is the equivalent of weak inversion in a MOS transistor. For a single gate JFET, this is typically done by computing a pinchoff value V_p for the control (i.e., gate to source) voltage V_{gs} and then in the model for operation when the transistor is not pinched off, replacing this by an effective control voltage $V_{gs}-n\phi_t \ln\{1+\exp[(V_{gs}-V_p)/n\phi_t]\}$, where n is a subthreshold swing parameter and $\phi_t = kT/q$ is the thermal voltage. This gives a logarithmic dependence on the control voltage in pinchoff. However, the situation is more complex for a dual-gate JFET.

Source pinchoff for dual-gate JFETs can be viewed in several ways. For a given source to bottom-gate voltage V_{sb}, there is a value for the source to top-gate voltage V_{st} that will cause pinchoff at the source end, and vice versa. In this view, there are two pinchoff voltages, one for each gate, each a function of the other gate voltages [2]. These can be handled through empirical intermediate values in an empirical model [2], which is unphysical and inaccurate, or by computing separate effective voltages for both V_{sb} and V_{st} [3], which increases model computation complexity.

An alternative approach [4] is to directly formulate I_{ds} in terms of a conducting channel thickness computed based on the average values of V_{sb} and V_{st} along the channel, which is equivalent to the mid-point-linearization model of [1]. However, this is again an empirical, and because the linearization of the square root is only exact at the channel mid-point potential, it does not accurately model the onset of pinchoff at the source, so overestimates the amount of depletion pinching at the source except for $V_{ds} = 0$. In fact, source pinchoff should be computed at $V_{ds} = 0$, and it should not be calculated based on the mid-point-linearized conducting channel thickness when $V_{ds} > 0$. Furthermore, this approach is not verified for MOS gates and it is not applicable to the exact, more accurate, dual-gate JFET model of [1].

A substantially simpler viewpoint is possible: instead of considering the bottom- and/or top-gate voltage as being so low that the channel is pinched off at the source, consider the source voltage as getting pulled high enough so that source pinchoff occurs. Source pinchoff can then be implemented with a single effective voltage calculation, rather than two. Furthermore, the source pinchoff voltage calculation is the same for both the exact and mid-point-potential linearization models for I_{ds}. This is the viewpoint we adopt in this paper. Source pinchoff is included in the model of [5]; however, this is to prevent numerical evaluation problems and is not done in a manner that accurately models I_{ds} when the source is pinched off.

The source pinchoff voltage V_{sp} is then a function of both the bottom- and top-gate voltages, V_b and V_t, respectively,[2] and we analyze the phase diagram of the solution space and develop a smooth analytical model for V_{sp}. Furthermore, in source pinchoff, there is no real saturation voltage V_{dsat} for the drain–source voltage, rather I_{ds} has a $1-\exp(-V_{ds}/\phi_t)$ dependence on V_{ds}, so has an effective saturation value of the thermal voltage ϕ_t. Our V_{sp} model is constructed to asymptotically have this behavior.

This paper presents our analysis of the phase space of V_{sp} as a function of V_b and V_t, and presents a solution for V_{sp} that is valid for any gate bias values and asymptotically has $V_{dsat}\to\phi_t$ in source pinchoff. From this, we develop an I_{ds} model valid for any operating region, nonsaturation, saturation (i.e., drain pinchoff), and source pinchoff, and verify it by comparison with numerical simulations. Models for drain-induced barrier lowering (DIBL) and channel-length modulation (CLM), which are necessary to accurately fit data from short-channel transistors, are also detailed.

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[1] Defined as which of the terminals labeled source and drain, for an n-channel JFET, has the most negative bias.

[2] Note that, although at first, this looks to reference voltages to ground, in the violation of the best practices detailed in [6]; if an arbitrary voltage is added to both V_b and V_t, then V_{sp} increases by the same amount, as we will show in Section II, so there is no issue.

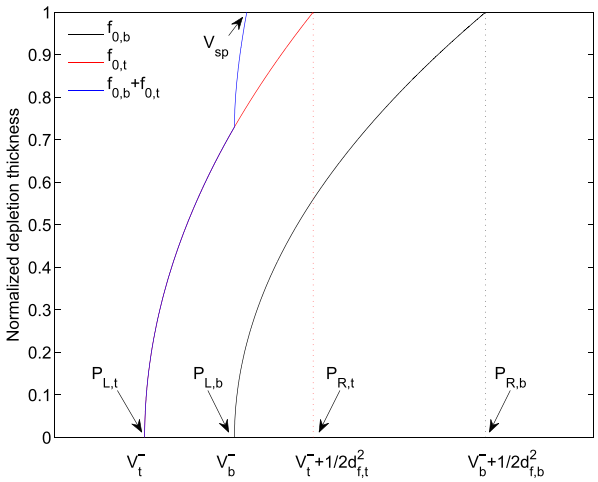

Fig. 1. $f_{0,b}$ and $f_{0,t}$ versus V_s. V_{sp} is the value of V_s at which $f_{0,b} + f_{0,t} = 1$. For the specific biases of V_b^- and V_t^- in this plot, V_{sp} falls within the interval $[V_b^-,\ V_t^- + 1/(2d_{f,t}^2)]$.

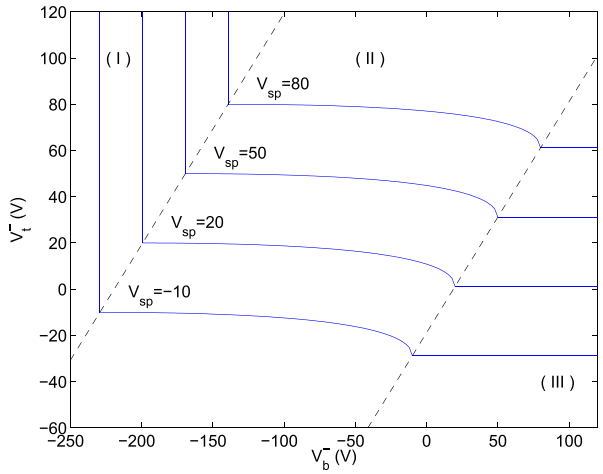

Fig. 2. Phase transition diagram of a dual p-n junction gate JFET. Solid lines: V_{sp} contours. Dashed lines: phase boundaries. The boundary between regions I and II is $V_t^- = V_b^- + 1/(2d_{f,b}^2)$. The boundary between regions II and III is $V_b^- = V_t^- + 1/(2d_{f,t}^2)$.

II. Source Pinchoff Voltage and Phase Diagram

We consider an n-channel dual-gate JFET [1, Fig. 1]. The exact solution for I_{ds}, when the source is not pinched off, is given by

$$I_{ds} = G_f \frac{1 - f_b - f_t}{\mu_{red}(\overline{E})} V_{ds} \tag{1}$$

where f_b and f_t are given in [1, eq. (9)]. If the mid-point-potential linearization approximation is used, then f_b and f_t are replaced by $\tilde{f}_b$ and $\tilde{f}_t$, respectively, of [1, eq. (11)].

V_{sp} is the value of the source voltage at which $1 - f_b - f_t = 0$ for $V_{ds} = 0$. That is

$$1 - f_{0,b}(\psi_b) - f_{0,t}(\psi_t) = 0 \tag{2}$$

where

$$\begin{aligned} f_{0,b}(\psi_b) &= d_{f,b}\sqrt{\psi_b} = d_{f,b}\sqrt{2}\sqrt{V_{sp} - V_b^-} \\ f_{0,t}(\psi_t) &= d_{f,t}\sqrt{\psi_t} = d_{f,t}\sqrt{2}\sqrt{V_{sp} - V_t^-} \end{aligned} \tag{3}$$

and

$$V_b^- = V_b - \psi_{r,b}/2, \quad V_t^- = V_t - \psi_{r,t}/2. \tag{4}$$

All the other symbols have the same meaning as in [1]. It is important to note that (2) applies, with no approximation, to both the exact and mid-point-linearization solutions for I_{ds}, because it is defined, and computed, at $V_{ds} = 0$.

The possible solution space for V_{sp}, as a function of V_b^- and V_t^-, is where the arguments of the square root terms in (3) are nonnegative and the quantities $f_{0,b}$ and $f_{0,t}$ are <1. Fig. 1 shows $f_{0,b}$ and $f_{0,t}$ as the functions of V_s for a pair of specific V_b^- and V_t^- biases. $f_{0,b} = 0$ at the point $P_{L,b}$, where $V_s = V_b^-$, and increases to 1 as V_s approaches the point $P_{R,b}$, where $V_s = V_b^- + 1/(2d_{f,b}^2)$. Similarly, $f_{0,t} = 0$ at the point $P_{L,t}$, where $V_s = V_t^-$, and increases to 1 as V_s approaches the point $P_{R,t}$, where $V_s = V_t^- + 1/(2d_{f,t}^2)$.

We need to examine the feasibility region, which is akin to a phase transition diagram, in (V_b^-, V_t^-) space to find the solution (see Fig. 2), in which constant V_{sp} contours are the solid lines. There are three regions. If $P_{L,t}$ is to the right of $P_{R,b}$, i.e., if $V_t^- > V_b^- + 1/(2d_{f,b}^2)$, then this is region I in Fig. 2. Here, the top-gate voltage is so high that when the channel is fully depleted at the source by the reverse biased bottom-gate voltage, then the depletion thickness due to the top gate is zero. Similarly, if $P_{L,b}$ is to the right of $P_{R,t}$, i.e., $V_b^- > V_t^- + 1/(2d_{f,t}^2)$, then this is region III in Fig. 2. Here, the bottom-gate voltage is so high that when the channel is fully depleted at the source by the reverse biased top-gate voltage, then the depletion thickness due to the bottom gate is zero. The rest of the (V_b^-, V_t^-) space is region II where both bottom and top gates deplete the channel. JFETs are designed to operate in region II. In regions I and III, one of the gate p-n junctions is forward biased so deeply that its junction barrier vanishes; therefore, the gate junction and the gate-channel-gate vertical bipolar transistor dominate the current–voltage characteristics of the overall transistor. Our model is based on channel depletion approximation, and is only accurate for region II. However, our model is numerically robust for all regions.

In region II of Fig. 2, both bottom and top gates deplete the channel. Solution of (2) for V_{sp} gives

$$V_{sp} = \frac{2\hat{h}}{\hat{g} + \sqrt{\hat{d}}} + \frac{V_b^- + V_t^-}{2} \tag{5}$$

where

$$\begin{aligned} \hat{d} &= 64 d_{f,b}^2 d_{f,t}^2 (1 + 2\hat{u}) \\ \hat{g} &= 4\left(d_{f,b}^2 + d_{f,t}^2\right)(1 + \hat{u}) \\ \hat{h} &= 1 + 2\hat{u} + \left(d_{f,b}^2 + d_{f,t}^2\right)^2 \left(V_b^- - V_t^-\right)^2 \\ \hat{u} &= \left(d_{f,b}^2 - d_{f,t}^2\right)\left(V_b^- - V_t^-\right). \end{aligned} \tag{6}$$

Note that $\hat{d}$, $\hat{g}$, $\hat{h}$, and $\hat{u}$ are the functions of the voltage difference $V_b^- - V_t^-$. Therefore, from the second term in (5),

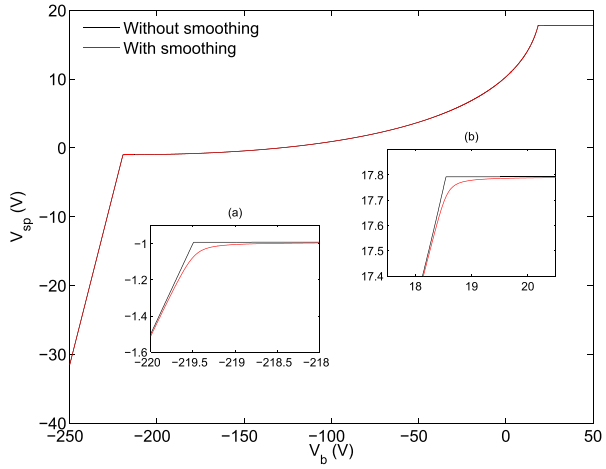

Fig. 3. $V_{\rm sp}$ versus V_b for $V_t = 0$. Insets: smooth behavior at the phase transition boundaries.

if both V_b^- and V_t^- are increased by some arbitrary amount, then $V_{\rm sp}$ increases the same amount, as should be the case.

As noted above, in practice, JFETs operate in region II of Fig. 2. However, for numerical robustness, the calculation of $V_{\rm sp}$ needs to be well behaved for all biases, including in regions I and III. We achieve this by clamping V_b^- and V_t^- at the region boundaries, as shown in Fig. 2. In region I, $P_{L,t}$ is to the right of $P_{R,b}$, so $V_{\rm sp}$ should be clamped at $P_{R,b}$. In region III, $P_{L,b}$ is to the right of $P_{R,t}$, so $V_{\rm sp}$ should be clamped at $P_{R,t}$. The clamping is done in a C^∞-continuous manner using

$$V_b^- \rightarrow \text{MINA}\left(V_b^-, V_t^- + \frac{1}{2d_{f,t}^2}, \hat{\delta}\right)$$
$$V_t^- \rightarrow \text{MINA}\left(V_t^-, V_b^- + \frac{1}{2d_{f,b}^2}, \hat{\delta}\right) \quad (7)$$

where (adapted from [7])

$$\text{MINA}(x, y, o) = \frac{1}{2}\cdot\left[x + y - \sqrt{(x-y)^2 + o^2}\right] \quad (8)$$

and $\hat{\delta}$ is a smoothing parameter.

Using the transformed V_b^- and V_t^- of (7) in (5) and (6) gives a smooth and continuous solution for $V_{\rm sp}$ over the whole (V_b^-, V_t^-) space, respectively. Fig. 3 shows $V_{\rm sp}$ as a function of V_b when $V_t = 0$, for both $\hat{\delta} = \phi_t$ (with smoothing) and $\hat{\delta} = 0$ (without smoothing). The insets expand the view around the cusp points at the phase transition boundaries.

In region II, where (7) guarantees, we operate

$$\hat{u} \geq -1/2 \quad (9)$$

(see the Appendix for a proof). This ensures that $\hat{g}$ and $\hat{d}$ of (6) are both positive, and hence, the solution of (5) is numerically robust.

III. Core $I_{\rm ds}$ Model Formalism

Two issues must be addressed to complete the core $I_{\rm ds}$ model: ensuring numerical robustness and ensuring that $V_{d\rm sat} \rightarrow \phi_t$ in source pinchoff.

A. Exact Solution for I_{ds}

For numerical robustness, the arguments of the square root terms in (3) need to be prevented from becoming negative. This is done by clamping them to a value $V_{\rm CL}$ with a smoothing parameter ϵ via

$$\underline{\psi}_b(V_s) = \text{MAXA}(\psi_{r,b} + 2V_s - 2V_b, V_{\rm CL}, \epsilon)$$
$$\underline{\psi}_t(V_s) = \text{MAXA}(\psi_{r,t} + 2V_s - 2V_t, V_{\rm CL}, \epsilon) \quad (10)$$

where [7]

$$\text{MAXA}(x, y, o) = \frac{1}{2}\cdot\left[x + y + \sqrt{(x-y)^2 + o^2}\right]. \quad (11)$$

$V_{\rm CL}$ is effectively the minimum potential difference across the p-n junction barrier under strong forward bias, and, in practice, we set this to 10^{-12} V.

As a consequence of the clamping, the smoothed $V_{\rm sp}$ is no longer a solution to (2). This issue is resolved by modifying (2) to become

$$U - f_{0,b}[\underline{\psi}_b(V_s)] - f_{0,t}[\underline{\psi}_t(V_s)] = 0 \quad (12)$$

where

$$U = f_{0,b}[\underline{\psi}_b(V_{\rm sp})] + f_{0,t}[\underline{\psi}_t(V_{\rm sp})]. \quad (13)$$

U is larger than but close to 1. Clearly, $V_{\rm sp}$ is a solution to (12).

Following the BSIM3 technique to smoothly transition between weak and strong inversions [8], our final core model for $I_{\rm ds}$ is:

$$I_{\rm ds} = G_f \frac{P_l}{P_s}\frac{P_h}{\mu_{\rm red}(\overline{E})}V_{\rm ds,eff}. \quad (14)$$

Here

$$P_l = U - f_{0,b}[\underline{\psi}_b(V_{s,e})] - f_{0,t}[\underline{\psi}_t(V_{s,e})]$$
$$P_s = U - f_{0,b}[\underline{\psi}_b(V_{s,\phi})] - f_{0,t}[\underline{\psi}_t(V_{s,\phi})]$$
$$P_h = U - f_b[\underline{\psi}_b(V_{s,\phi})] - f_t[\underline{\psi}_t(V_{s,\phi})] \quad (15)$$

and

$$V_{s,e} = V_{\rm sp} - n\phi_t \ln\left[1 + \exp\left(\frac{V_{\rm sp} - V_s}{n\phi_t}\right)\right]$$
$$V_{s,\phi} = V_{\rm sp} - \phi_t - n\phi_t \ln\left[1 + \exp\left(\frac{V_{\rm sp} - \phi_t - V_s}{n\phi_t}\right)\right] \quad (16)$$

where n is a model parameter that controls the slope of $\partial \ln I_{\rm ds}/\partial V_s$ in source pinchoff.

P_l and P_h control the behavior below and above source pinchoff, respectively. P_s functions as a selector. When $V_s > V_{\rm sp}$, the source is pinched off, and P_l approaches zero exponentially and P_h/P_s approaches 0.5. This gives the desired overall exponential dependence of $I_{\rm ds}$ on V_s in source pinchoff operation. When $V_s < V_{\rm sp}$, the source is not pinched off, $P_l \approx P_s$, and P_h approaches the original $1 - f_b - f_t$ term in (1) because $V_{s,\phi} \approx V_s$. This gives the desired behavior and the original $I_{\rm ds}$ model of [1, eq. (8)], when the source is not pinched off.

To calculate $V_{d\rm sat}$, we first factor U out of P_h, which leads to $d_{f,b} \rightarrow d_{f,b}/U$ and $d_{f,t} \rightarrow d_{f,t}/U$, then we follow the method given in [1]. Because $V_{s,\phi}$ limits to $V_{\rm sp} - \phi_t$ instead of $V_{\rm sp}$, from [1, eqs. (9) and (11)], we have $V_{d\rm sp} \rightarrow \phi_t$. This means, from [1, eq. (27)], that $V_{d\rm sat} \rightarrow \phi_t$ in source pinchoff, as desired.

B. Mid-Point-Potential Linearization Solution for I_{ds}

The computation of quantities related to source pinchoff is done at $V_{ds} = 0$, where the exact and mid-point-potential linearization models for I_{ds} are identical. The computed V_{sp} and model (14), therefore, still apply, with the f_b and f_t terms replaced with the approximate forms $\tilde{f}_b$ and $\tilde{f}_t$, respectively.

IV. Additonal Model Details

Several additional physical phenonema need to be included in a practical model; these are detailed in this section and partially based on those of the R3 model [9]. Parasitic capacitance and, for p-n junction gates, leakage current are also included, but these are standard, so details are not provided here.

A. Channel-Length Modulation

When a transistor saturates, i.e., when the drain end of the channel is pinched off but the source end is not, the effective length of the channel is modulated by the drain voltage; as V_{ds} increases, the length of the drain pinchoff region increases, which decreases the effective channel length of the transistor and increases the value of the G_f factor in (1), thereby, increasing I_{ds}. To model this effect, we adopt the CLM models for MOS transistors from [10]

$$I_{ds} \rightarrow I_{ds} \cdot \{1 + c1[1 + c1c(V_{sp} - V_{s,e})]V_{ds}\} \cdot \{1 + c2[(V_{ds} + c2v)^{c2e} - c2v^{c2e}]\} \quad (17)$$

where c quantities are the parameters and the default value for the exponent $c2e$ is $1/2$. The first modifier represents a simple Early voltage-type term that gives a constant output conductance, and the square root form of the second modifier models how the length of the pinchoff depletion region at the drain end varies with V_{ds}.

B. Drain-Induced Barrier Lowering

In contrast to MOS transistors, in a JFET, there is no p-n junction barrier between the source and the channel, so at first, it would appear that the concept of DIBL would not be relevant. However, that is incorrect. When the channel is depleted, i.e., in source pinchoff, the gates pull up the channel potential, thereby creating a potential barrier between the channel and the source. Fig. 4 shows the conduction band edge along the channel between the source and the drain for dual-gate JFETs, operating in source pinchoff, with $L = 2$ and 10 μm. The solid curves for $V_{ds} = 0.1$ V show a source-to-channel barrier of $\sim$1 V. When V_{ds} is increased to 15 V, the barrier in the long device is unaffected; but for the short device, the barrier is significantly lowered. JFETs are, therefore, such as MOS transistors, affected by DIBL.

DIBL is implemented in R3 by lowering the effective source voltage. However, that approach does not work for dual-gate JFETs because the lowered source voltage can cause one of the gate junctions to become forward biased. Therefore, we implement DIBL by lowering the depletion factors as

$$d_{f,t} \rightarrow d_{f,t} - d2t[(V_{ds} + d2v)^{d2e} - d2v^{d2e}]$$
$$d_{f,b} \rightarrow d_{f,b} - d2b[(V_{ds} + d2v)^{d2e} - d2v^{d2e}] \quad (18)$$

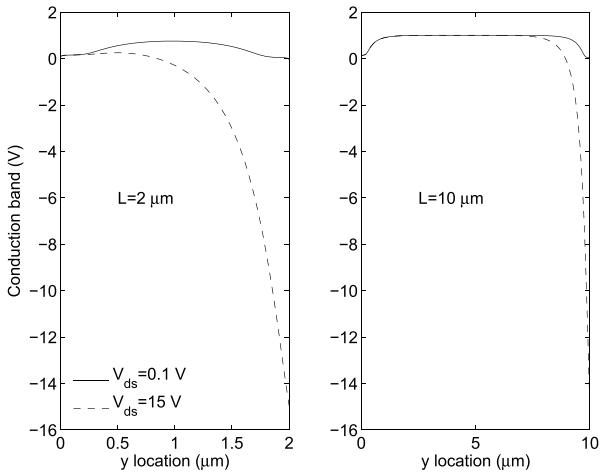

Fig. 4. TCAD simulation of the conduction band edge in the middle of the channel from source to drain for dual p-n junction gate JFETs biased in source pinchoff. $V_t = V_b = -11$ V and $V_s = 0$ V.

where d quantities are the parameters. Typically, the DIBL effect saturates at high V_{ds}.

C. Minimum Channel Conductance

When a transistor is biased deep in source pinchoff, the channel conductance can become affected by imprecision in floating-point computations, and may even become negative. To maintain reasonable behavior under such conditions, we add a small minimum conductance in parallel with the channel, so

$$I_{ds} \rightarrow I_{ds} + G_f g_{rpo} V_{ds} \quad (19)$$

where g_{rpo} is the parameter that specifies a minimum relative conductance to use in source pinchoff; 10^{-14} is a reasonable value for systems using double-precision floating-point numbers.

V. Comparison With TCAD Data

To verify our model, we compare it with transfer and output characteristic curves from TCAD simulations [11], for JFETs with both dual p-n junction gates and one p-n junction gate and one MOS gate. For the dual p-n junction gate structure, the simulated dual-gate JFET had top- and bottom-gate doping concentrations of 10^{20} and 10^{16} cm^{-3}, respectively, with a channel doping of 10^{17} cm^{-3} and a metallurgical channel thickness of 0.5 μm. We only give results from the exact I_{ds} model; the decrease in accuracy when using the mid-point-potential linearization approximation was presented in [1]. Velocity saturation was included in the TCAD simulations, and they were done at a temperature of 300 K.

Figs. 5 and 6 show the transfer characteristic curves, on linear and log-linear scales, respectively, when both gates are tied together, for low and high V_{ds}. The accuracy of modeling of both the source pinchoff voltage and the smooth transition to where a conducting channel exists is clear. The leakage current, apparent in the TCAD results for large negative gate biases, was not included in the compact model simulations to

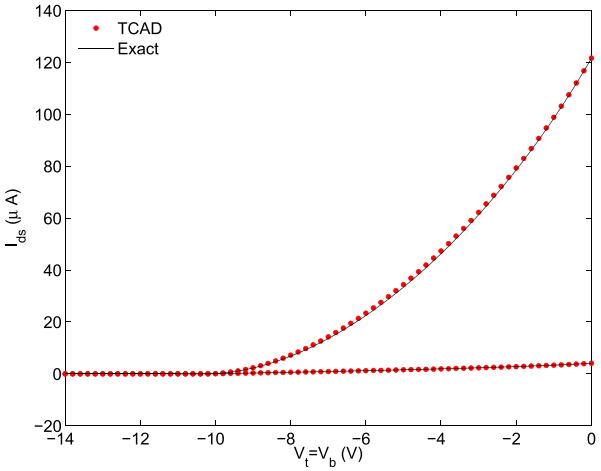

Fig. 5. Transfer characteristic curves of a dual p-n junction gate JFET. $W = 1$ μm. $L = 10$ μm. $V_t = V_b$. $V_d = 0.1$ V (lower curve). $V_d = 15$ V (upper curve). $V_s = 0$.

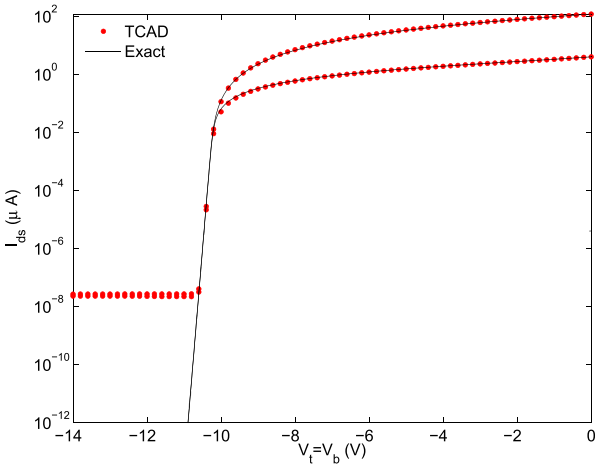

Fig. 6. Curves from Fig. 5 on a log-linear scale.

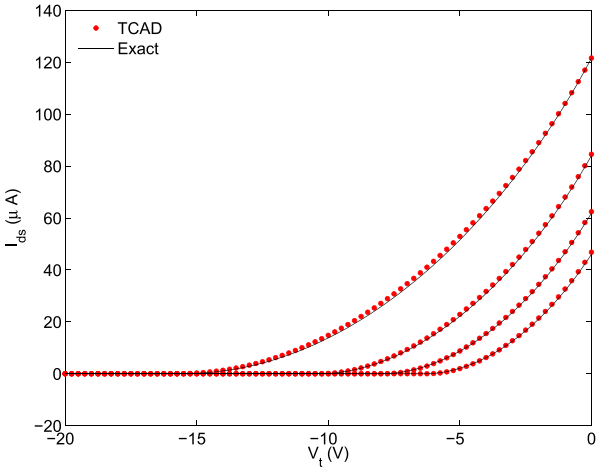

Fig. 7. Top-gate transfer characteristic curves of a dual p-n junction gate JFET. $W = 1$ μm. $L = 10$ μm. $V_b = 0, -10, -20$, and -30 V (left to right). $V_d = 15$ V. $V_s = 0$.

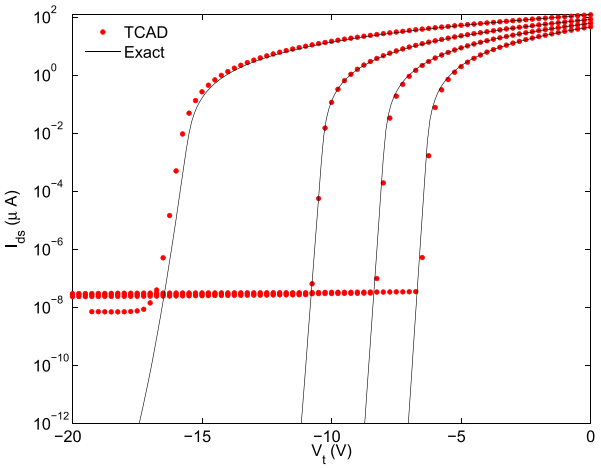

Fig. 8. Curves from Fig. 7 on a log-linear scale.

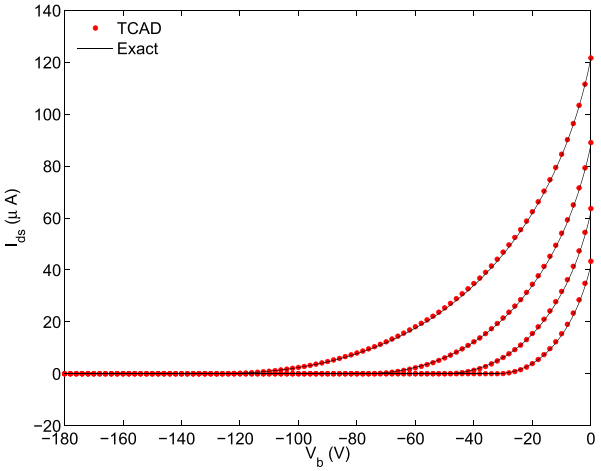

Fig. 9. Bottom-gate transfer characteristic curves of a dual p-n junction gate JFET. $W = 1$ μm. $L = 10$ μm. $V_t = 0, -2, -4$, and -6 V (left to right). $V_d = 15$ V. $V_s = 0$.

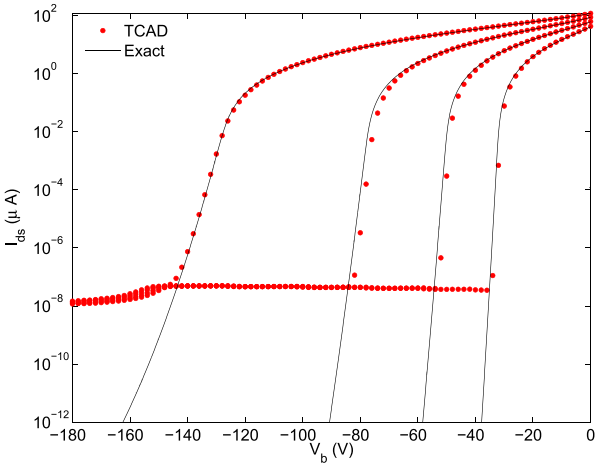

Fig. 10. Curves from Fig. 9 on a log-linear scale.

highlight the accuracy and numerical robustness of our core model down to very low currents.

Figs. 7 and 8 show the transfer characteristic curves with respect to V_t, on linear and log-linear scales, respectively, for $V_b = 0, -10, -20$, and -30 V and $V_{\rm ds} = 15$ V. Similarly, Figs. 9 and 10 show the transfer characteristic curves with respect to V_b, on linear and log-linear scales, respectively, for $V_t = 0, -2, -4$, and -6 V and $V_{\rm ds} = 15$ V. Our source pinchoff model smoothly and accurately reproduces the

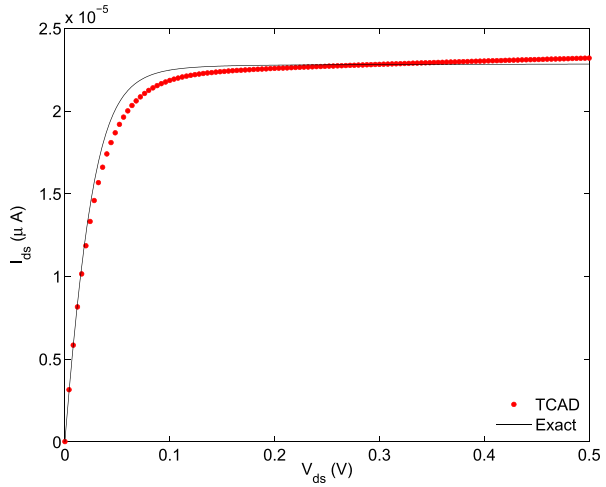

Fig. 11. Output characteristics curve of a dual p-n junction gate JFET under source pinchoff. $W = 1$ μm. $L = 10$ μm. $V_s = 0$. $V_t = V_b = -10.4$ V.

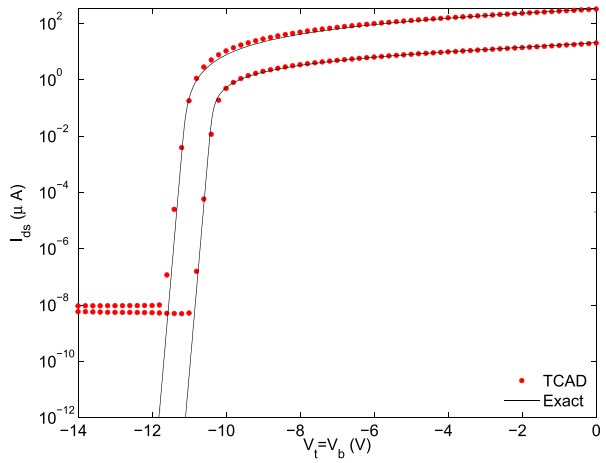

Fig. 12. Transfer characteristic curves of a dual p-n junction gate JFET. $W = 1$ μm. $L = 2$ μm. $V_t = V_b$. $V_d = 0.1$ V (lower curve). $V_d = 15$ V (upper curve). $V_s = 0$.

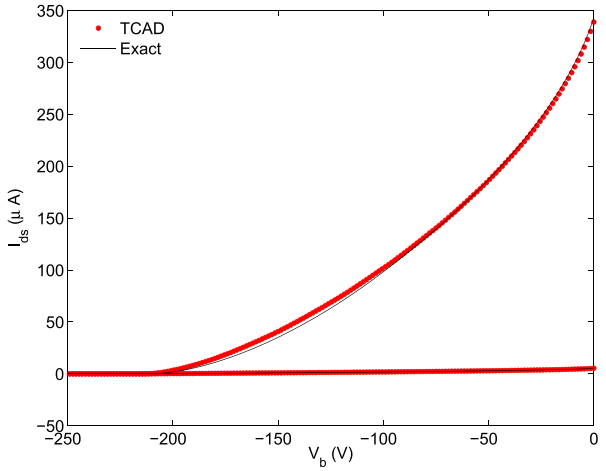

Fig. 13. Transfer characteristic curves of a JFET with one p-n junction gate and one MOS gate. $W = 1$ μm. $L = 10$ μm. $V_t = 0$. $V_d = 0.1$ V (lower curve). $V_d = 15$ V (upper curve). $V_s = 0$.

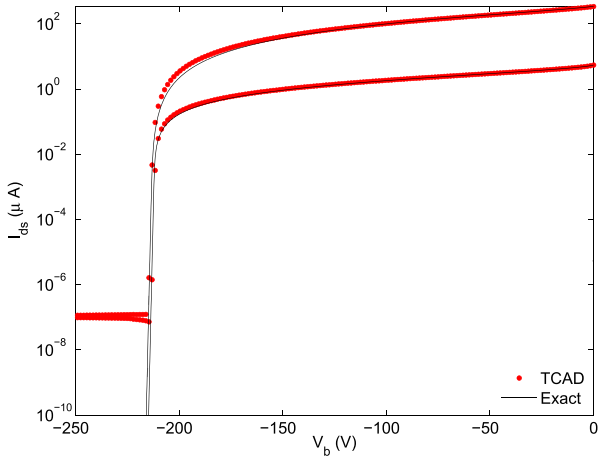

Fig. 14. Curves from Fig. 13 on a log-linear scale.

TCAD data over a wide range of applied biases, including the effects of significant asymmetry between top- and bottom-gate doping concentrations.

Fig. 11 shows an output characteristic curve for a dual p-n junction gate JFET biased in source pinchoff. Although not perfect, the accuracy with which our model approximates the $1 - \exp(-V_{ds}/\phi_t)$ behavior is clear; this also verifies the accuracy of our V_{dsat} model and the calculation under source pinchoff, when $V_{dsat} \to \phi_t$. Note that δ in [1, eq. (32)] should be set to $2\phi_t$.

Fig. 12 shows the transfer characteristic curves on log-linear scales for a dual p-n junction gate JFET with a channel length of 2 μm and both gates tied together. The DIBL effect is significant and is modeled well; $d2t = 5.16 \times 10^{-3}$, $d2b = 1.81 \times 10^{-2}$, $d2v = 0$, and $d2e = 0.5$.

Figs. 13 and 14 show the transfer characteristic curves, on linear and log-linear scales, respectively, for the JFET with one p-n junction gate and one MOS gate. The MOS gate is grounded. The channel and bottom-gate parameters are the same as for the dual p-n junction gate case, and $t_{ox,t} = 400$ nm. Again, the accuracy of modeling of both the source pinchoff voltage and the smooth transition to where a conducting channel exists is clear. The MOS gate cannot pinchoff the channel, because to do so would require the surface under that gate to become inverted; that situation is not captured by our model.

VI. Conclusion

We have developed a source pinchoff voltage model for dual-gate JFETs by analyzing the phase diagram of pinchoff as a function of V_b and V_t. From this, we developed a complete I_{ds} model valid for all biases that smoothly transitions to, and has $V_{dsat} \to \phi_t$ in, source pinchoff operation. Our model was verified by comparison with numerical simulations. In practice, nonideal aspects of the model were also discussed.

Appendix

Here, we prove inequality (9) in Section II. The boundary conditions of region II ensure that

$$V_b^- - V_t^- \geq -\frac{1}{2d_{f,b}^2} \tag{20}$$

$$V_b^- - V_t^- \leq \frac{1}{2d_{f,t}^2}. \tag{21}$$

Now, if $d_{f,b}^2 > d_{f,t}^2$, multiply (20) by $d_{f,b}^2 - d_{f,t}^2$ to give

$$\hat{u} \geq -\frac{d_{f,b}^2 - d_{f,t}^2}{2d_{f,b}^2} = -\frac{1}{2} + \frac{d_{f,t}^2}{d_{f,b}^2} \geq -\frac{1}{2}. \tag{22}$$

If $d_{f,b}^2 < d_{f,t}^2$, multiplying (21) by $d_{f,b}^2 - d_{f,t}^2$ gives

$$\hat{u} \geq \frac{d_{f,b}^2 - d_{f,t}^2}{2d_{f,t}^2} = \frac{d_{f,b}^2}{d_{f,t}^2} - \frac{1}{2} \geq -\frac{1}{2}. \tag{23}$$

If $d_{f,b}^2 = d_{f,t}^2$, $\hat{u} = 0 > -1/2$. Therefore, (9) holds for all possible values of $d_{f,b}$ and $d_{f,t}$.

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