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A User Guide on the

Flexible Transition Metal Dichalcogenide Field-Effect Transistor (TMDFET) Verilog-A Model

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TMDFET model implementation based on the work of [1].

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1. Model Files

Table 1. Summary of Files

File Name		**Description**
	tmdfetn_v_1_0_0.va	N-type TMDFET Verilog-A model definition.
	tmdfetp_v_1_0_0.va	P-type TMDFET Verilog-A model definition.
benchmark/	gates_mos2.lib	Gates and circuits definition library.
	technology.lib	Suggested design parameters.
	mos2_XXX_spice_delay.sp	*inv*, *nand*2, *nor*2, *nand*3, *nor*3, *nand*4, *xor*2, 7-stage FO4 buffer chain, and *c*17 benchmark circuits netlist.
test/	tmdfet_sample.sp	Example HSPICE netlist using the above model.
references/	TMDFET-ASPDAC16.pdf	Publication the TMDFET model is based on.
TMDFET_userguide_v_1_0_0.pdf		This file

This manual provides a basic outline of the TMDFET model and the input definitions needed for HSPICE simulations.

2. Scope of the Model

Table 2 below summarizes the scope of the model.

Table 2. Summary of the Scope of the TMDFET Model

Device Types	n-type/p-type TMDFET
Device Dimensions:	
Channel Length (Minimum)	~15nm
Channel Length (Maximum)	~100nm
Channel Width (Minimum)	~15nm
Channel Width (Maximum)	~500nm
Top Oxide Thickness (Minimum)	1nm
Top Oxide Thickness (Maximum)	20nm
Bottom Oxide Thickness (Minimum)	1nm
Bottom Oxide Thickness (Maximum)	100nm
Strain (Minimum)	0%
Strain (Maximum)	100%

This model was designed for TMDFET devices (See Figure 1). The minimum channel length is ~15nm, as various complex quantum mechanisms which describe the sub-15nm regime are not modeled here.

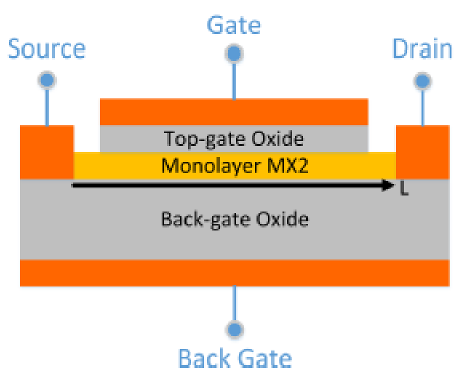

Figure 1. Illustration of Modeled TMDFET Device.

3. Model Usage

This section illustrates how to instantiate the model in HSPICE.

3.1 Model Instantiation

To instantiate the devices in the model, the library must be included at the beginning of the SPICE deck in the following way:

```
.hdl "tmdfetn_v_1_0_0.va"
.hdl "tmdfetp_v_1_0_0.va"
```

The above library files contains the following models:

tmdfetnmos	n-type TMDFET model.
tmdfetpmos	p-type TMDFET model.

Modifications should not be done in the model definition files (e.g. tmdfetn_v_1_0_0.va). All changes in device and global parameters should be done in the “technology.lib”.

The syntax to instantiate a TMDFET is given below.

*Top level n-type TMDFET Standard Model:

XDevice *Drain Gate Source Sub* **tmdfetnmos** < *W*=32*n* *L*=16*n* *Tox*=2.8*n* *Tox2*=2.8*n* *strain*=0 >

*Top level p-type TMDFET Standard Model:

XDevice *Drain Gate Source Sub* **tmdfetpmos** < *W*=32*n* *L*=16*n* *Tox*=2.8*n* *Tox2*=2.8*n* *strain*=0 >

The TMDFET model definitions *Drain, Gate, Source and Sub* are same as that of standard MOSFET HSPICE models and also Predictive Technology Models (PTM). *Drain* and *Source* port definition are not interchangeable due to the equation definitions in the model. The assumption is that the drain voltage V_D is always greater or equal to the source voltage V_S. The *Substrate* (*Sub)* can also be used as the second gate or back gate in transistor model. By default, we set the substrate oxide thickness *Tox2*=100nm for single-gate devices.

The model assumes default parameter values when the parameters are not defined during usage. Table 3 contains the default values of parameter and their definitions.

Table 3. Device Parameter Definitions and Default Values

Device Parameter	Description	Default Value
L	Physical channel length.	16nm
W	Device width	32nm
Tox	The thickness of top gate dielectric material (planer gate).	2.8nm
Tox2	Oxide Thickness between channel and substrate/bottom gate	100nm
Strain	Applied strain (percent)	0

4. Global Parameters

The definition and values of those global parameters are summarized in Table 4. These parameters are used for internal computations in the model and can be changed by the user if so desired. These parameters cannot be modified for each TMDFET defined in the circuit.

Table 4. Global Parameter Definitions and Values

Global Parameters	Description	Default Value
P__q	Electron Charge in Coulomb	1.60217646e-19
P__h	Planck’s constant in J.s	6.62606896E-34
P__hbar	Reduced Planck’s constant in J.s	P__h/(2π)
P__k	Boltzmann’s constant in J/K	1.3806505E-23
P__pi	Value of π	3.14159265
P__eps	Permittivity in F/m	8.854187817E-12
P__T	Temperature in K	300
m0	Electron Mass in kg	9.10938291e-31

5. References

[1] Y-Y. Chen, M. Gholipour, and D. Chen, "Flexible Transition Metal Dichalcogenide Field-Effect Transistors: A Circuit-Level Simulation Study of Delay and Power under Bending, Process Variation, and Scaling," *IEEE/ACM Asia and South Pacific Design Automation Conference*, pp. 761-768, Jan. 2016.

6. Contacts and Website

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For the latest model file updates please visit:
http://dchen.ece.illinois.edu/.

The SPICE version of this model is available in nanoHUB: https://nanohub.org/resources/23426.
Please report any bugs to us. Suggestions and comments are also welcome. Thanks for downloading.