Fundamentals of Nanotransistors

Unit 4: Transmission Theory of the MOSFET

Lecture 4.8: Limits of MOSFETs

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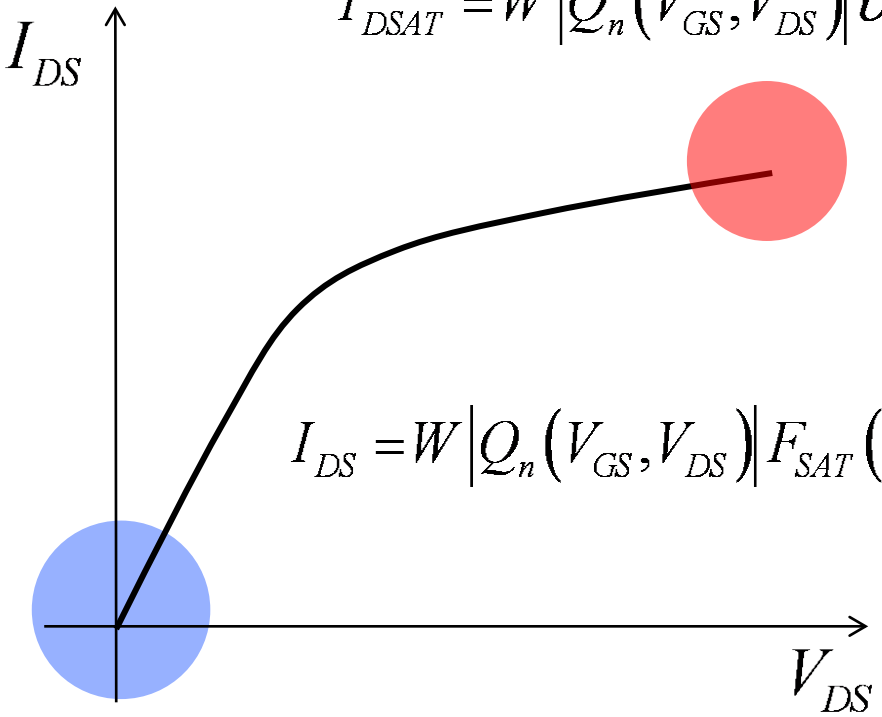
Transmission / VS model



$$I_{DSAT} = W\left|Q_n\left(V_{GS}, V_{DS}\right)\right|\upsilon_{inj}$$

$$I_{DS} = W\left|Q_n\left(V_{GS}, V_{DS}\right)\right|F_{SAT}\left(V_{DS}\right)\upsilon_{inj}$$

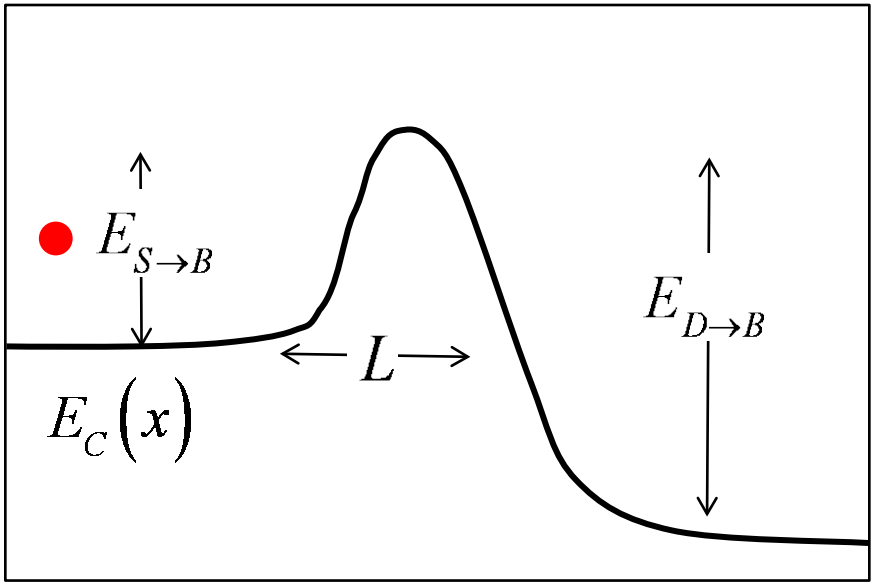
$$I_{DLIN} = \frac{W}{L}\mu_{app}\left|Q_n\left(V_{GS}, V_{DS}\right)\right|V_{DS}$$

1) What are the fundamental limits of MOSFETs?

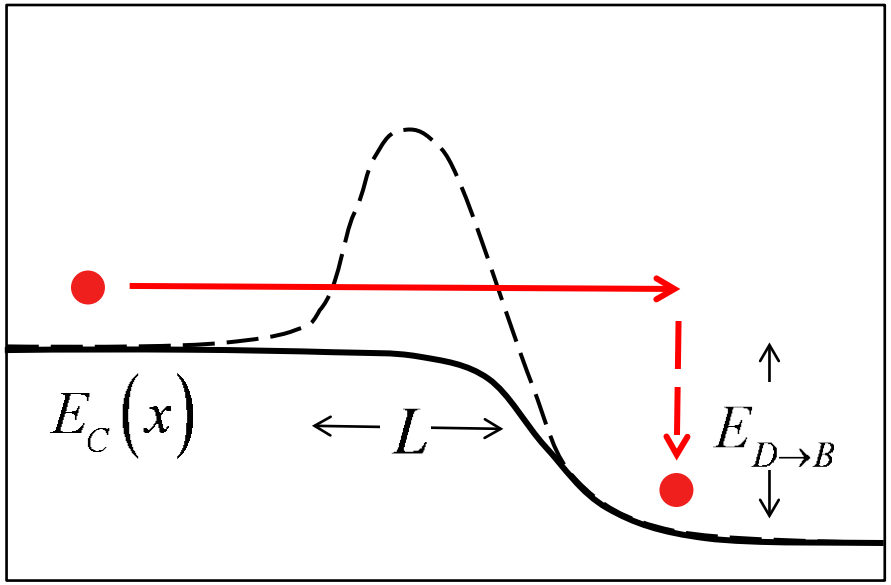
2) How close are we to those limits today?

MOSFETs are barrier controlled devices

Off-state



On-state



(Recall Lecture 1.5)

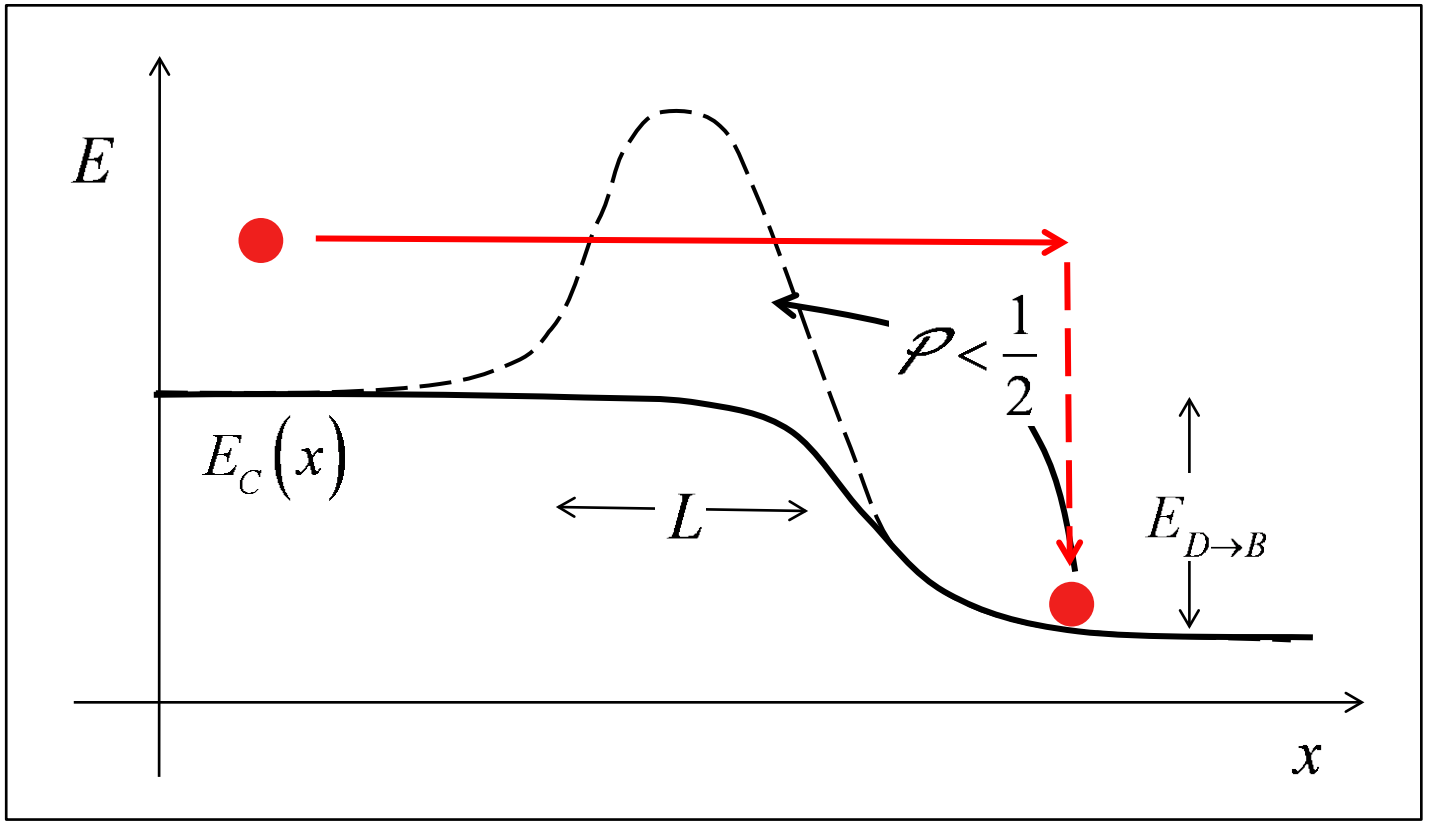
Fundamental limits of MOSFETs

We will use some very simple arguments to estimate some ultimate limits for transistors. Our approach is similar to (but not quite the same) as the approach of Zhirnov, et al.

V. V. Zhirnov, R.K. Cavin III, J.A. Hutchby, and G.I. Bourianoff, ”Limits to Binary Logic Switch Scaling – A Gedanken Model,” *Proc. IEEE*, **91**, pp. 1934 - 1939 , 2003.

Minimum switching energy

On-state



Minimum switching energy

$$\mathcal{P} = e^{-E_{D\to B}/k_B T}$$

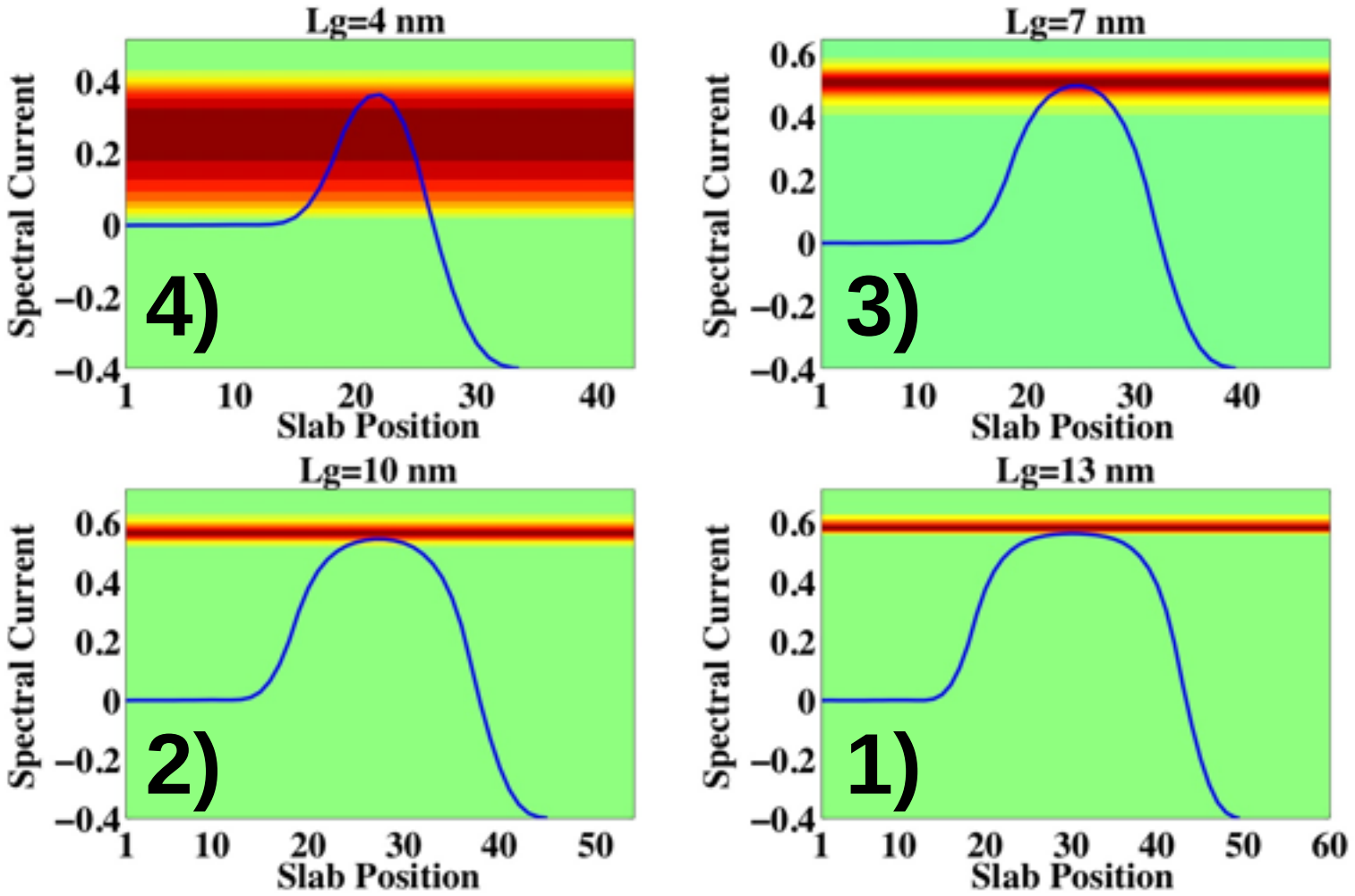
To have a switching event, the electron must stay in the drain and not be thermionically re-emitted back to the source. We require:

$$\mathcal{P} = e^{-E_{D\to B}/k_B T} < \frac{1}{2}$$

$$e^{-E_{\min}/k_B T} = \frac{1}{2}$$

$$E_{\min} = k_B T \ln 2$$

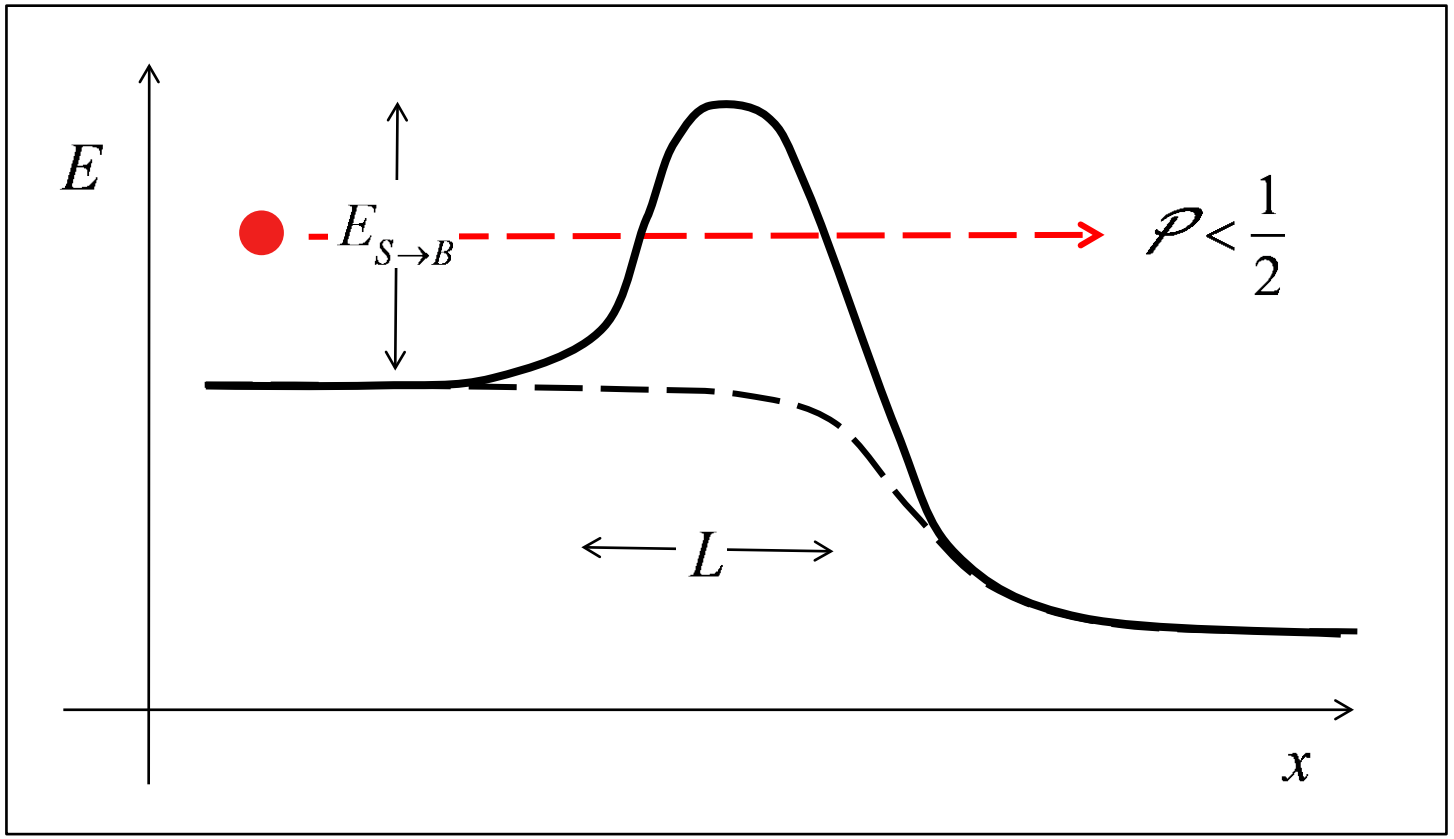
Minimum channel length and QM tunneling



(Provided by M. Luisier, ETH Zurich)

Minimum channel length

Off-state



Minimum channel length

$$\mathcal{P} = e^{-2\sqrt{2m^* E_{S\to B} L}/\hbar}$$ (WKB approximation)

$$\mathcal{P} < \frac{1}{2}$$ (To say that the device is off)

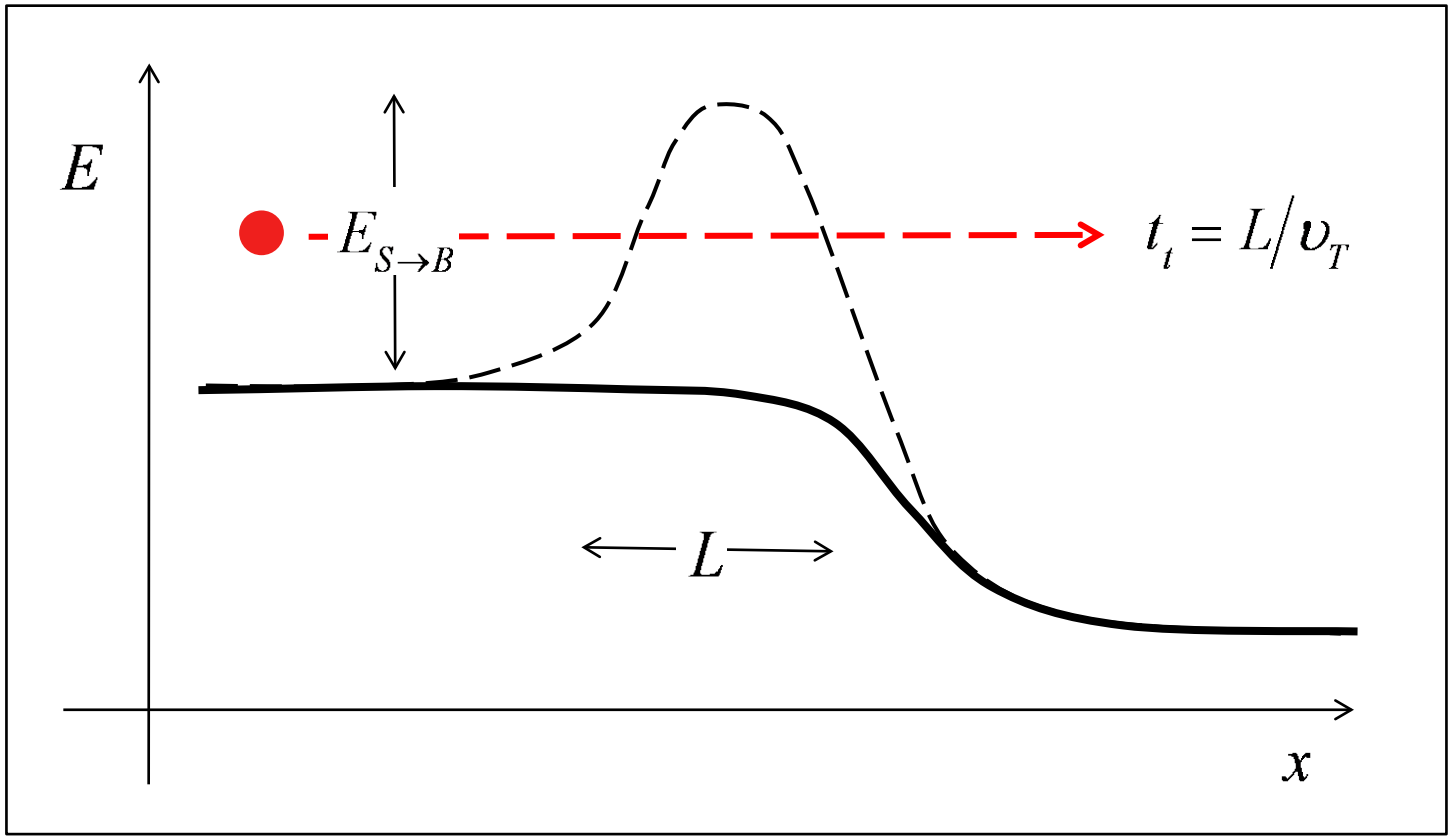
$$L > \frac{\hbar}{\sqrt{2m^* E_{S\to B} L}}$$

$$E_{S\to B} = E_{\min}$$

$$L_{\min} = \frac{\hbar}{\sqrt{2m^* E_{\min}}}$$

Minimum switching time

On-state



Minimum switching time

The minimum switching time is the **transit time** – the time it takes for an electron to cross the channel.

$$t_t = \frac{L}{\upsilon_T}$$

$$\tau_{\min} = \frac{L_{\min}}{\upsilon_T} \qquad \upsilon_T = \sqrt{\frac{2k_BT}{\pi m^*}} \qquad E_{\min} = k_BT\ln 2$$

(Discarding some constants on the order of unity…)

$$\tau_{\min} = \frac{\hbar}{E_{\min}}$$

“Fundamental limits”

$$E_{\min} = k_B T \ln 2 = 0.017 \text{ eV}$$

$$L_{\min} = \frac{\hbar}{\sqrt{2m^* E_{\min}}} = 1.5 \text{ nm} \qquad \left(m^* = m_0\right)$$

$$\tau_{\min} = \frac{\hbar}{E_{\min}} = 40 \text{ fs}$$

22 nm technology

$$V_{DD} = 0.7 \text{ V}$$

$$C_{inv} \approx 2.9 \times 10^{-6} \text{ F/cm}^2$$

$$C_G = C_{inv}(WL) \approx 0.6 \times 10^{-15} \text{ F}$$

$$W = 1\,\mu\text{m} \quad L = 22\,\text{nm}$$

$$I_{ON} \approx 1 \times 10^{-3} \text{ A}/\mu\text{m}$$

$$\frac{1}{2} C_G V_{DD}^2 \approx 57{,}000 \times E_{\min}$$

$$L = 20 \text{ nm} = 13 \times L_{\min}$$

$$\tau = \frac{C_G V_{DD}}{I_{ON}} \approx 11 \times \tau_{\min}$$

Channel length and switching time are within about a factor of 10 above fundamental limits. Energy (and power) are orders of magnitude larger that the fundamental limits.

Summary

1) Transistors are approaching some fundamental limits.

2) Practical, technology considerations such as series resistance, parasitic capacitance, BTBT leakage currents, etc. are likely to set the practical limits.

3) Good transistors behave semiclassically and operate by thermionic emission with voltage-controlled barrier heights.

4) Our semi-classical, “essential physics” model may well describe barrier controlled transistors forever.