Fundamentals of Nanotransistors

Unit 2: MOS Electrostatics

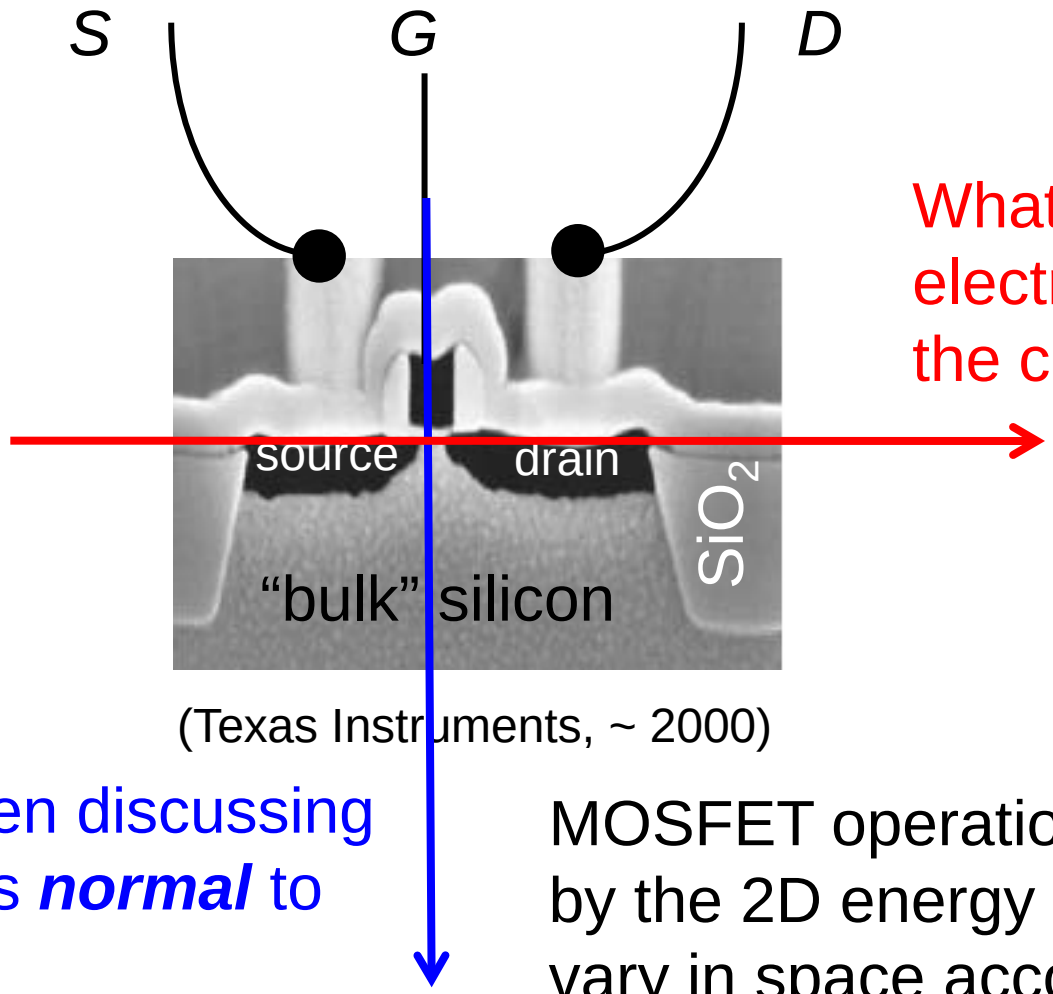
Lecture 2.7: 2D MOS Electrostatics

Mark Lundstrom

lundstro@purdue.edu
Electrical and Computer Engineering
Birck Nanotechnology Center
Purdue University, West Lafayette, Indiana USA

PURDUE UNIVERSITY

Bulk MOSFETs



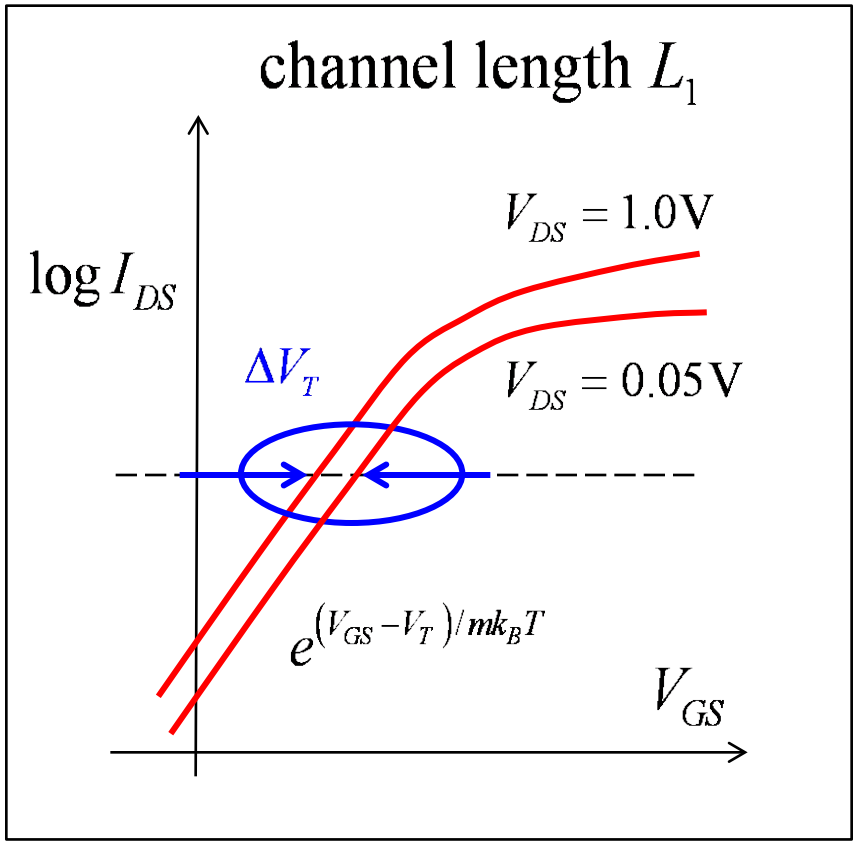
(Texas Instruments, ~ 2000)

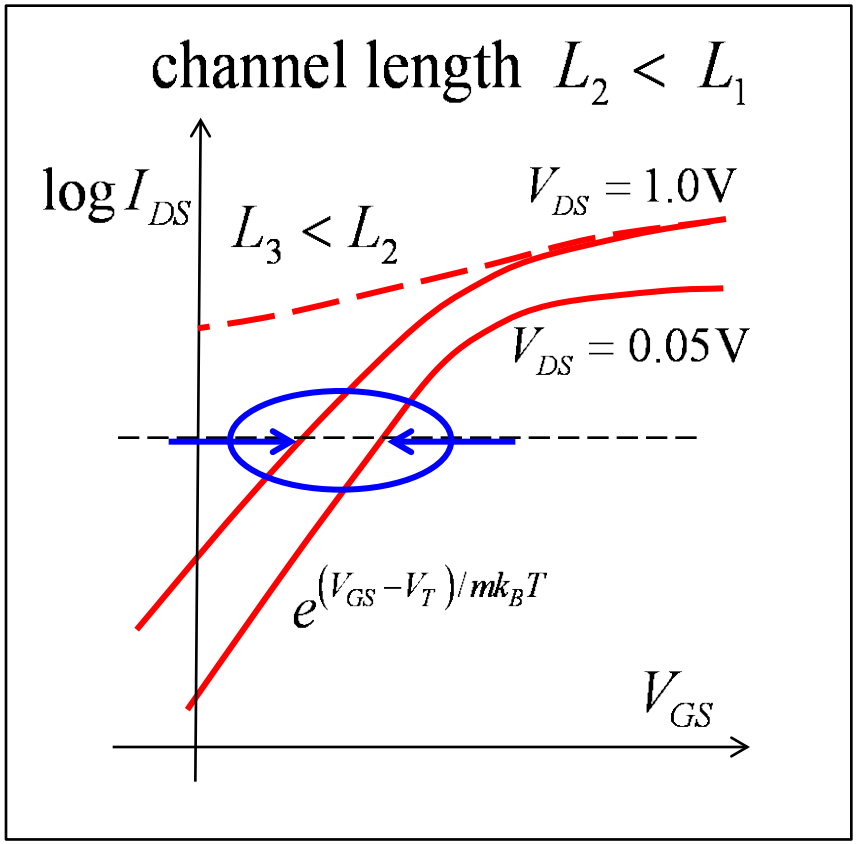
What about electrostatics ***along*** the channel?

We have been discussing electrostatics ***normal*** to the channel.

MOSFET operation is determined by the 2D energy bands, which vary in space according to the 2D electrostatic potential: $\psi(x,y)$

Effect of 2D electrostatics on I_{DS} vs. V_{GS}





1) DIBL increases with decreasing L and increasing V_{DS}
2) SS may increase with decreasing L and increasing V_{DS}
3) "Punchthrough" is a severe 2D effect.

2D Poisson equation

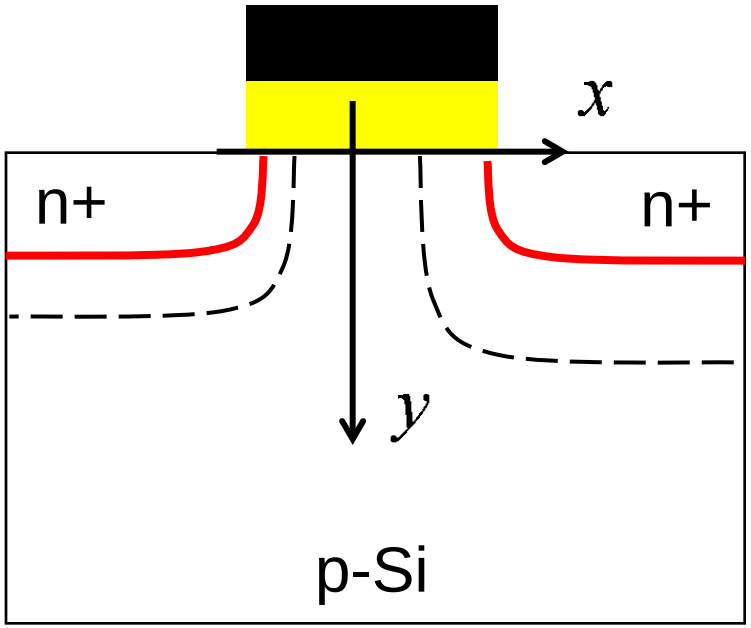
$$\nabla \bullet \vec{D}(x,y) = \rho(x,y)$$

$$\vec{D}(x,y) = \varepsilon_S \vec{\mathcal{E}}(x,y)$$

$$\vec{\mathcal{E}}(x,y) = -\vec{\nabla}\psi(x,y)$$

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_S}$$

2D Poisson equation



1) 1D MOS Capacitor:

$$\frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho}{\varepsilon_S} = \frac{qN_A}{\varepsilon_S} \quad (\text{below} V_T)$$

2) 2D MOSFET:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_S} \quad (\text{below} V_T)$$

"gradual channel approximation" $\frac{\partial^2 \psi}{\partial y^2} >> \frac{\partial^2 \psi}{\partial x^2}$ (long channel)

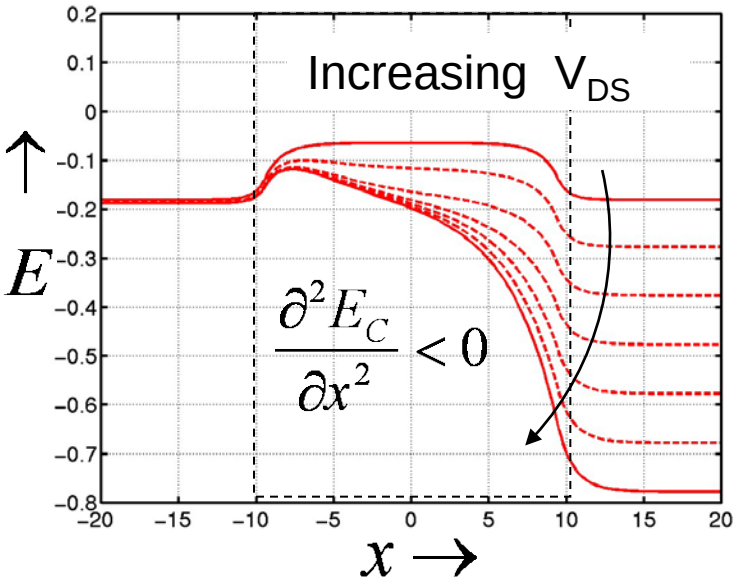
Understanding V_T reduction

1) Short channel MOSFET below threshold:

$$\frac{\partial^2 \psi}{\partial y^2} = \frac{qN_A}{\varepsilon_S} - \frac{\partial^2 \psi}{\partial x^2}$$

$$\frac{\partial^2 \psi}{\partial y^2} = \frac{q N_A\big|_{eff}}{\varepsilon_S}$$

$$N_A\big|_{eff} < N_A$$



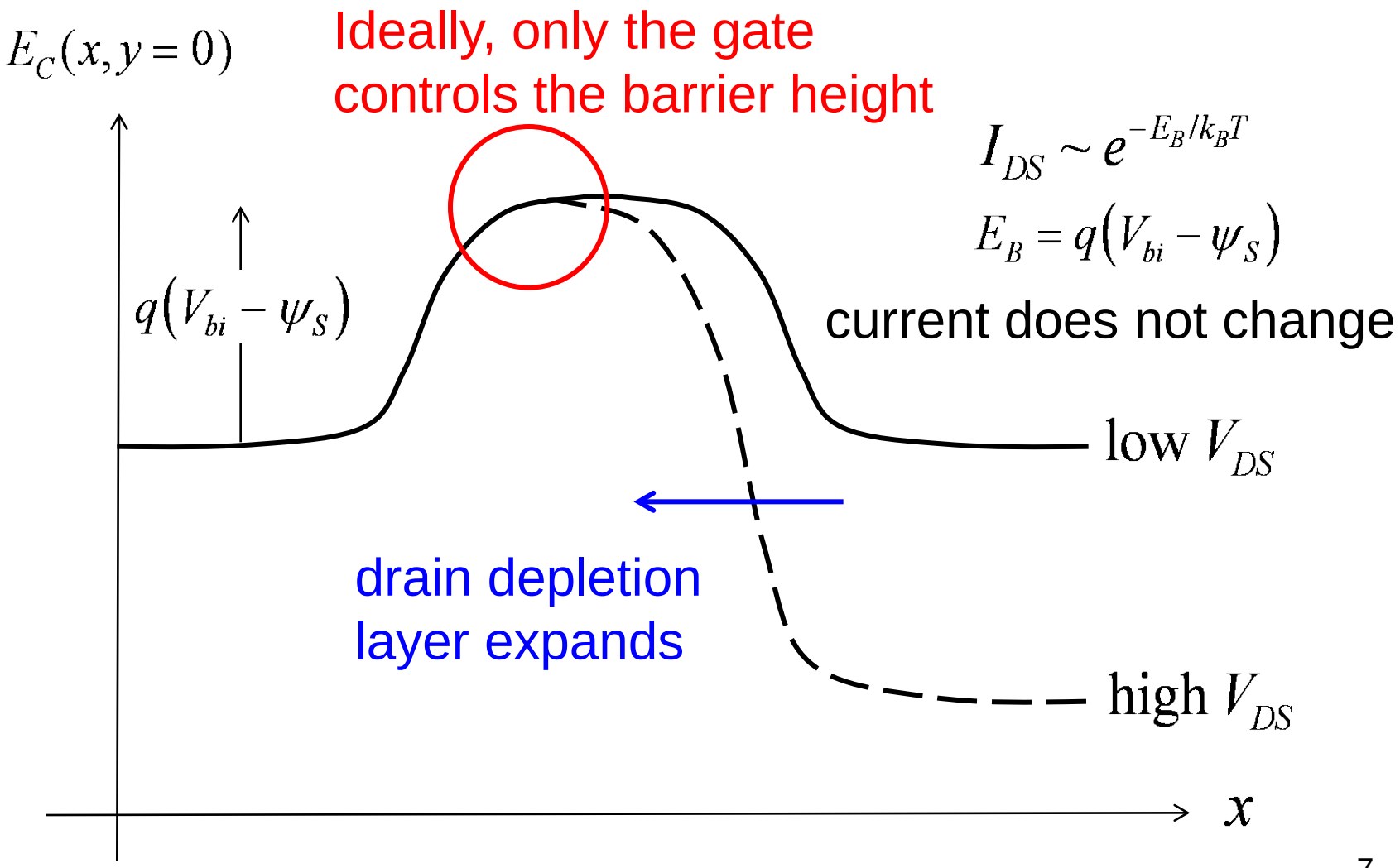
$$V_T = V_{FB} + \frac{\sqrt{2qN_A\varepsilon_S(2\psi_B)}}{C_{ox}} + 2\psi_B$$

(Lecture 2.3)

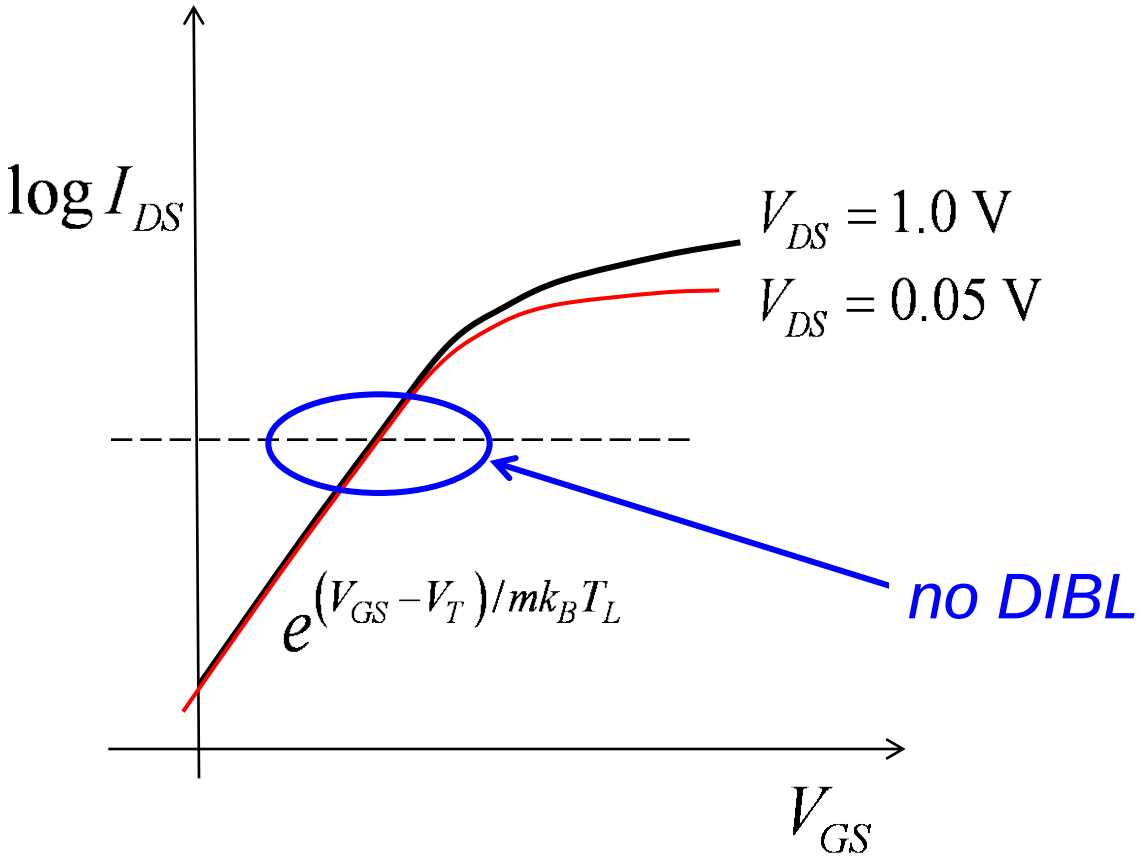
$$V_T < V_T(\text{long channel})$$

"explains" V_T roll-off

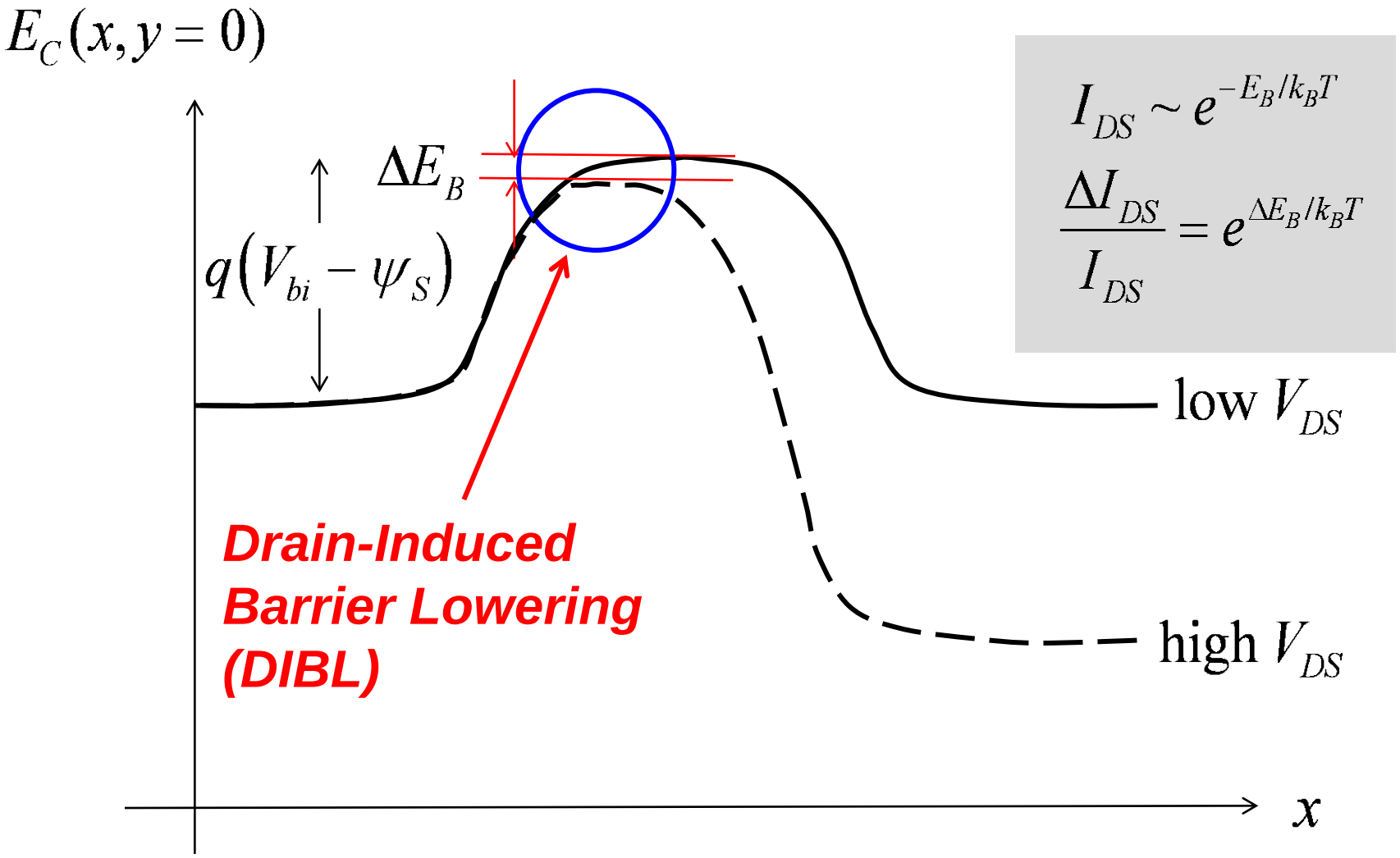
Barrier lowering view



No barrier lowering → no DIBL



Barrier lowering

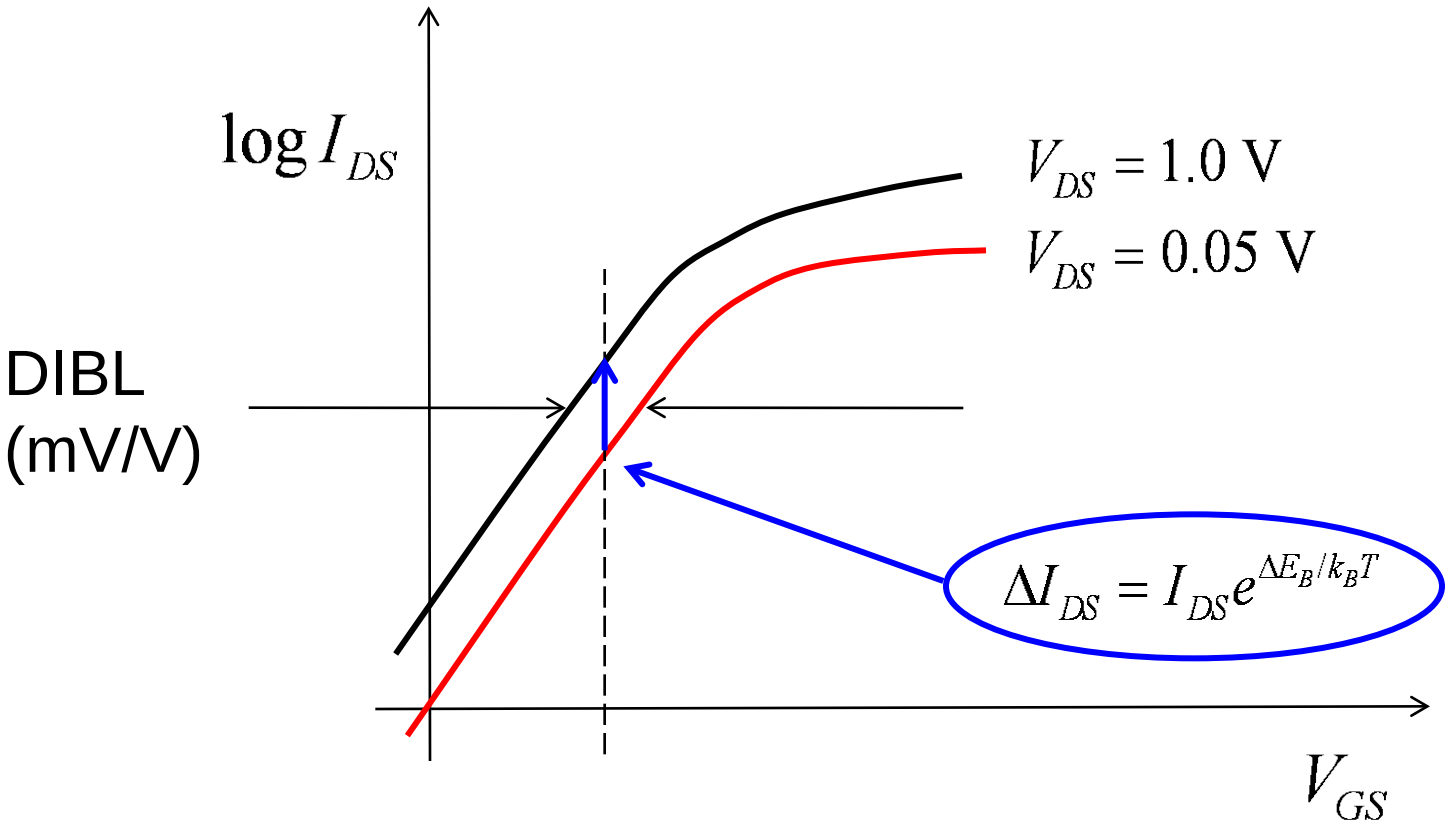


$$I_{DS} \sim e^{-E_B/k_BT}$$

$$\frac{\Delta I_{DS}}{I_{DS}} = e^{\Delta E_B/k_BT}$$

Drain-Induced Barrier Lowering (DIBL)

Barrier lowering increases current

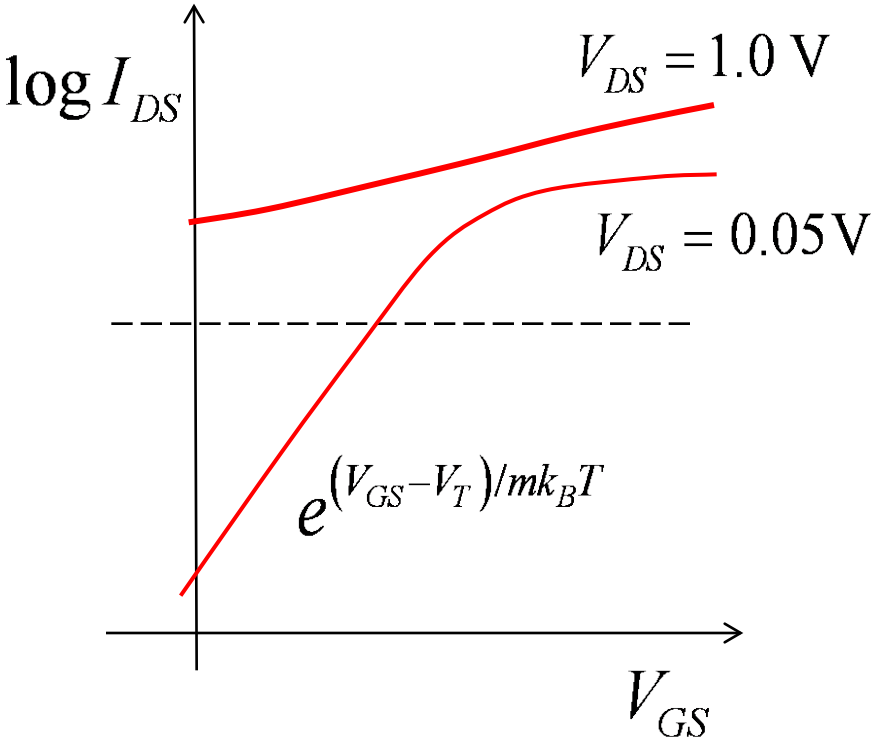


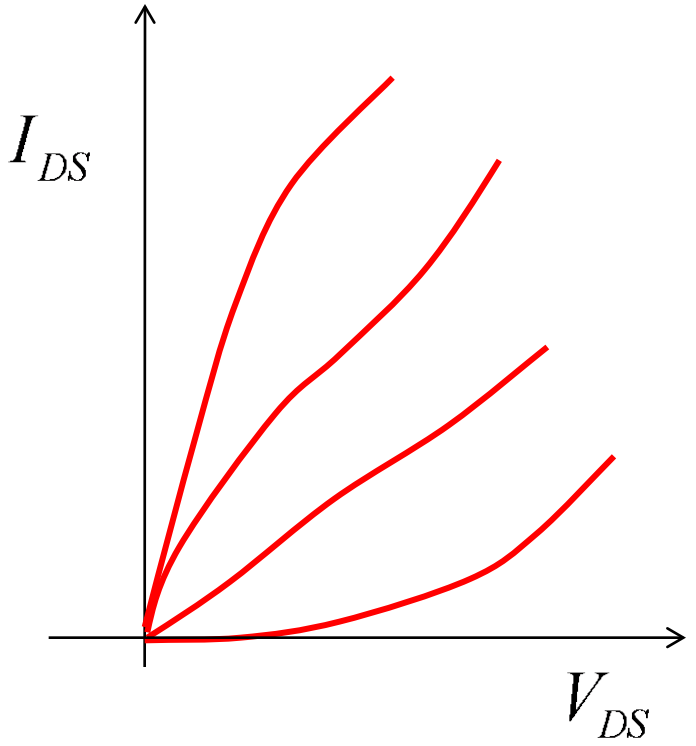
SS is still independent of $|V_{DS}|$.

Punchthrough

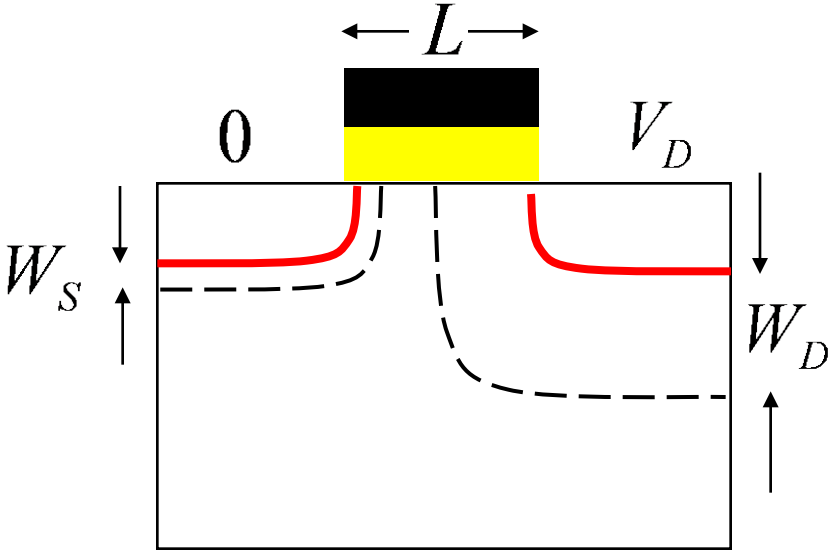
transfer

output



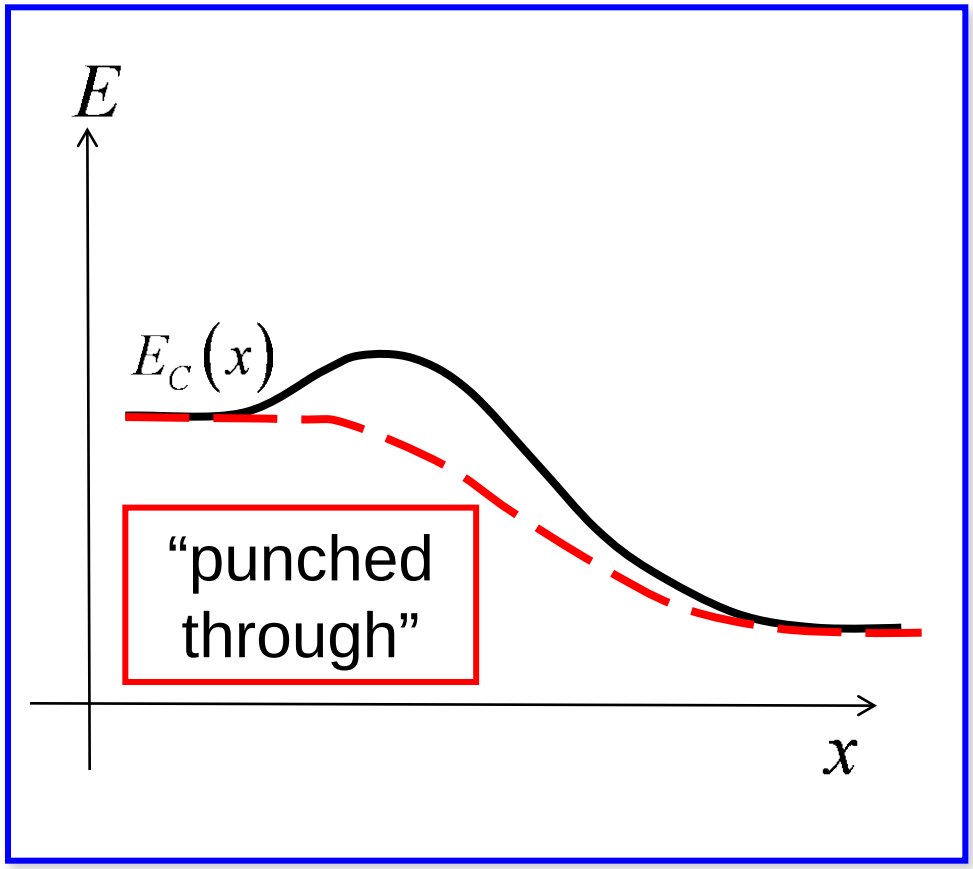


Punchthrough



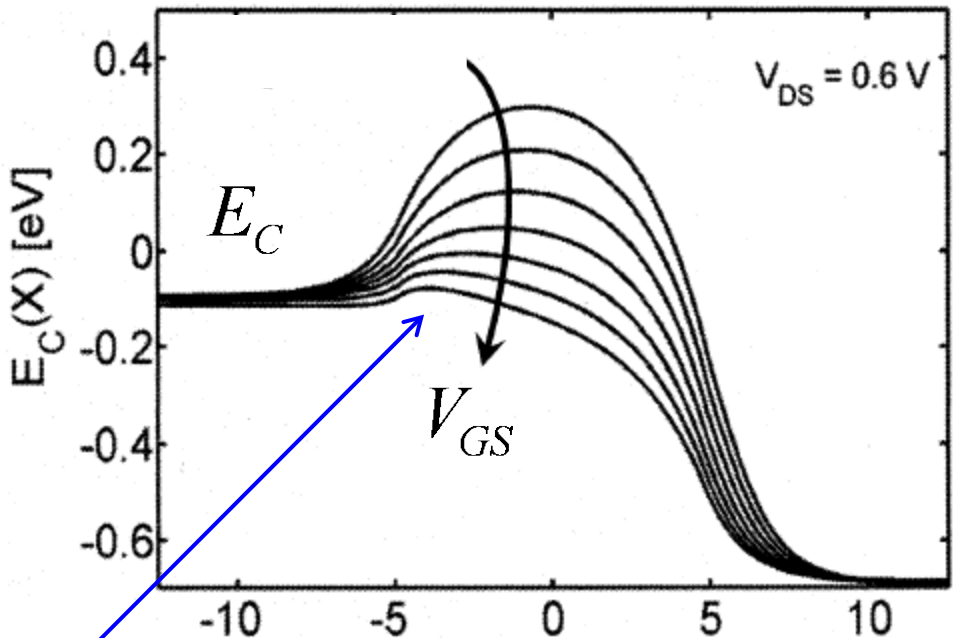
$$N_A(\min): \text{punch through}$$

$$W_S + W_D < L$$



A “well-tempered MOSFET”

(Dimitri Antoniadis, MIT)



The height of the barrier should be controlled by the gate voltage; the drain voltage should have only a small effect.

Controlling 2D electrostatics

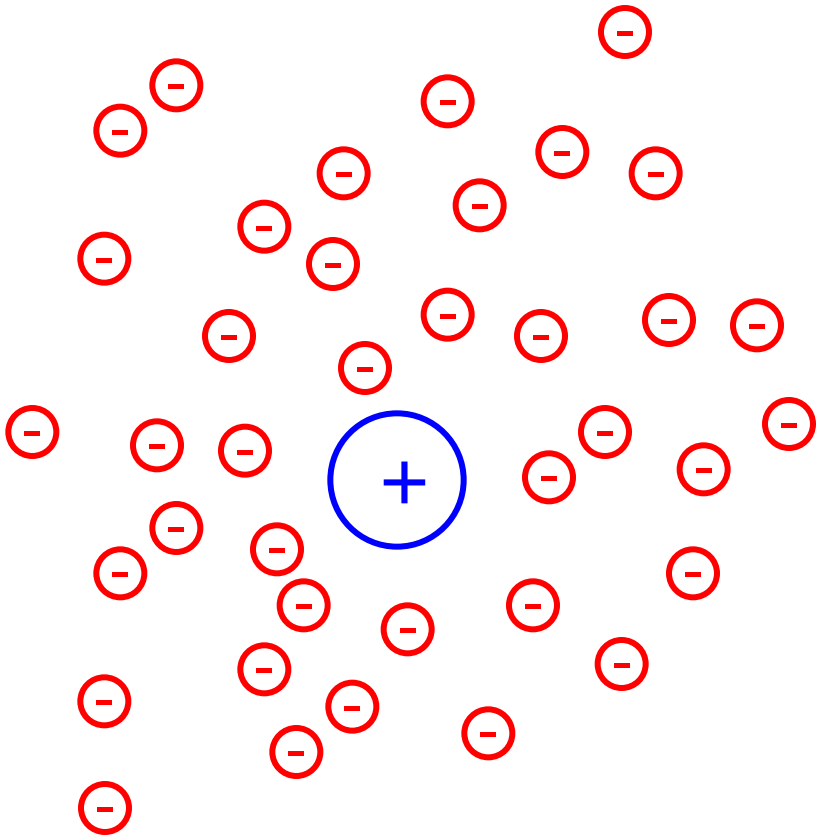
(also known as “short channel effects”)

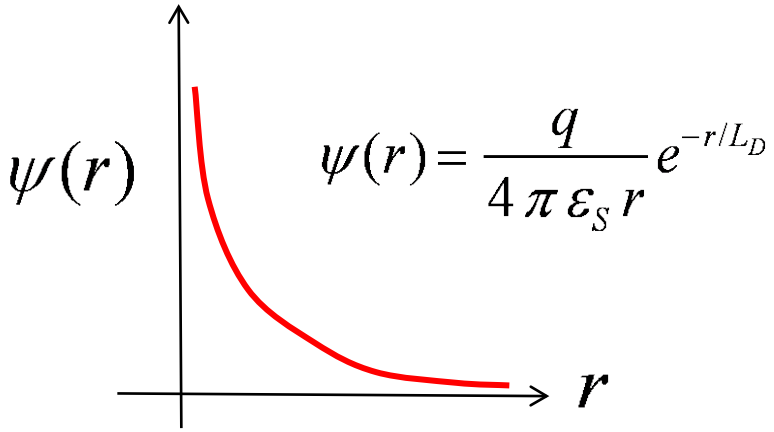
Need to design a short channel device to minimize 2D effects.

Question: How do we control 2D electrostatics in short channel MOSFETs?

Answer: Screen out the 2D fields.

Screening by free carriers



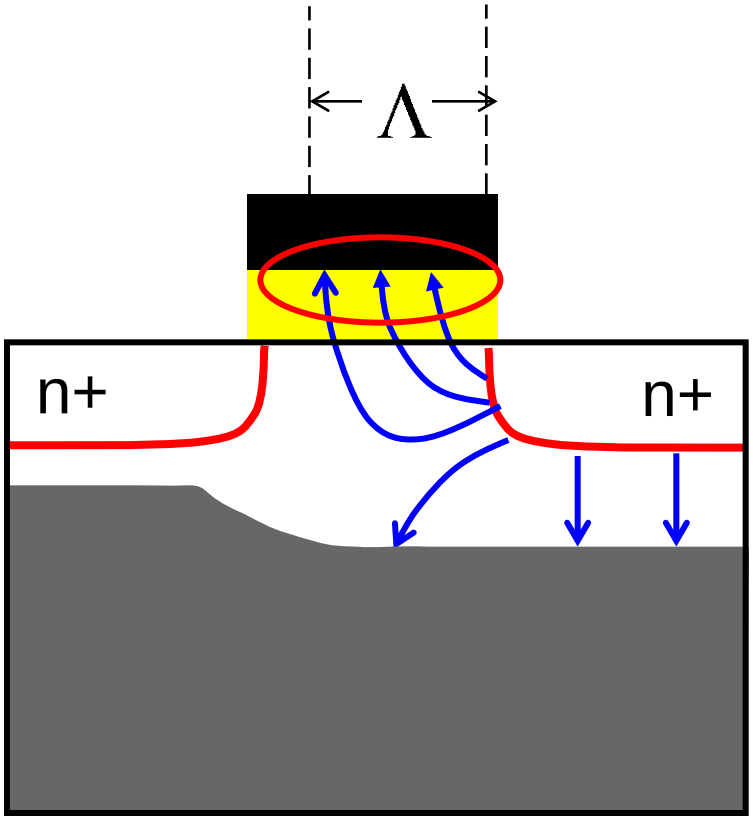


$$\psi(r) = \frac{q}{4\pi\varepsilon_S r} e^{-r/L_D}$$

$$L_D = \sqrt{\frac{\varepsilon_S k_B T}{q^2 n_0}}$$

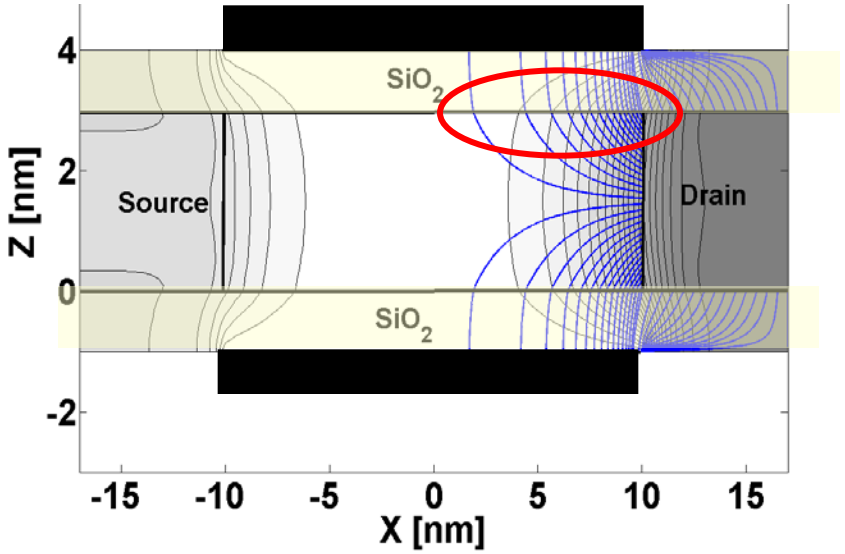
Debye length

Geometric screening length: bulk MOSFET



Geometric screening length: DG MOSFET

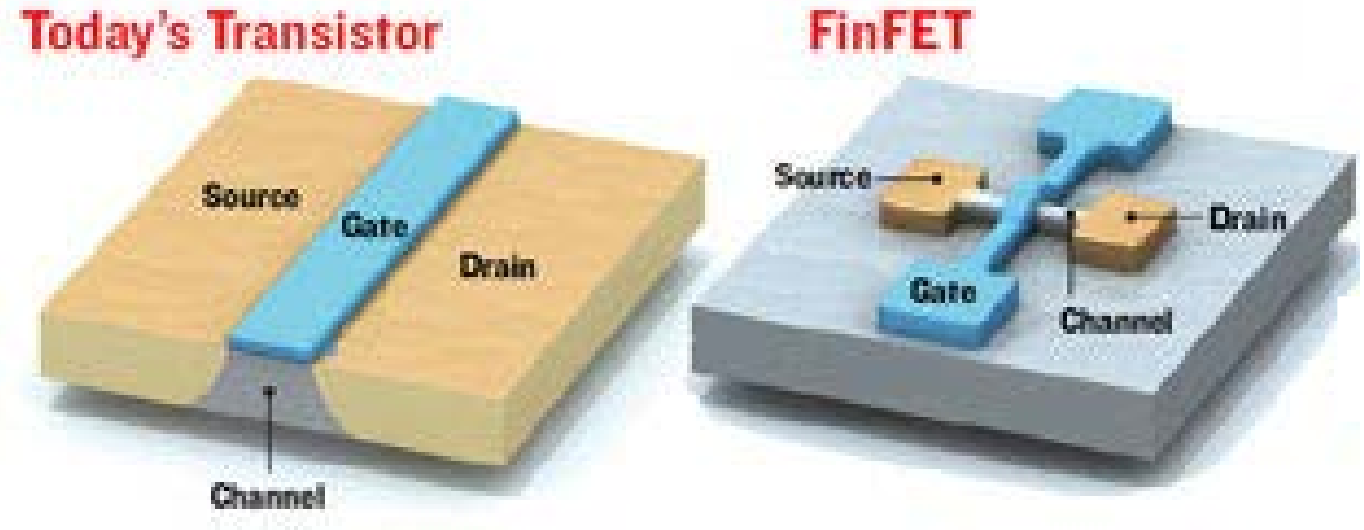
$\leftarrow \Lambda \rightarrow$



$$T_{OX} = 1\,\text{nm}$$

Off-state: $V_G = 0V$, $V_D = 1V$, $I_{off} = 0.1\mu A/\mu m$ (by H. Pal, Purdue, 2012)

Non-planar MOSFETs



"Transistors go Vertical," *IEEE Spectrum*, Nov. 2007.

See also: "Integrated Nanoelectronics of the Future," Robert Chau, Brian Doyle, Suman Datta, Jack Kavalieros, and Kevin Zhang, *Nature Materials*, **6**, 2007

Computing Λ

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_S} = \frac{-qN_A(x,y)}{\varepsilon_S}$$

$$\Lambda_{NW} < \Lambda_{DG\,SOI} < \Lambda_{SOI} < \Lambda_{BULK}$$

$$L_{\min} \approx 3\Lambda$$

D. J. Frank, Y. Taur, and H.-S. P.Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Lett*., **19**, pp. 385–387,1998.

Qian Xie, Jun Xu, and Yuan Taur, "Review and Critique of Analytic Models of MOSFET Short-Channel Effects in Subthreshold," *IEEE Trans. Electron Dev.*, **59**, pp 1569-1579, 2012.

2D electrostatics

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = \frac{-qN_A(x,y)}{\varepsilon_S}$$

1) Effective doping

2) Barrier lowering

3) Geometric screening length

4) Capacitor model (lecture notes)

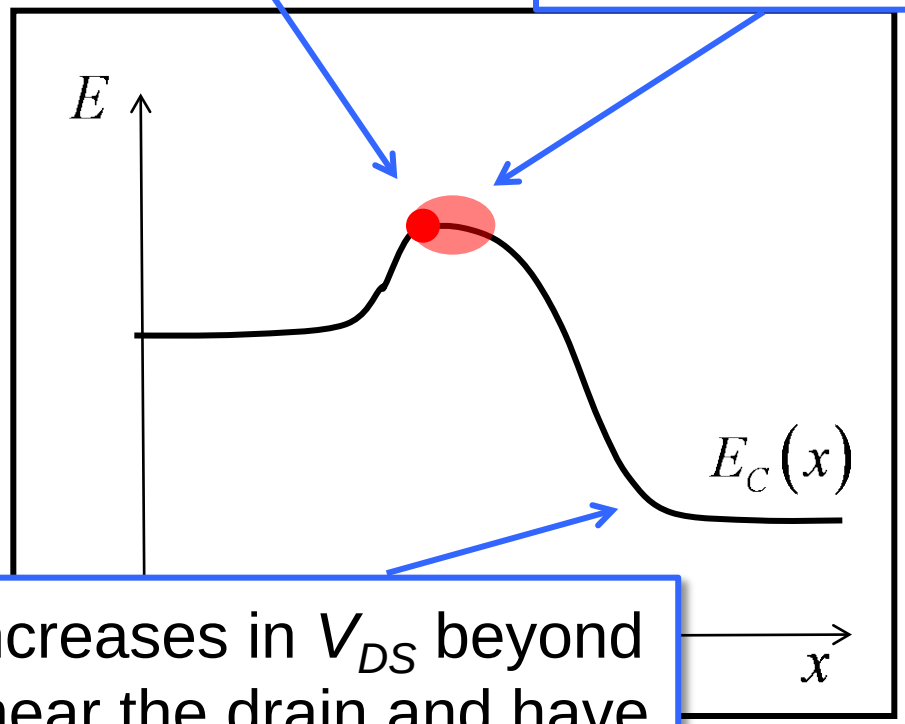
"Well-tempered MOSFET"

1) $Q_n(0) \approx -C_{inv}(V_{GS} - V_T)$

2) region under strong control of gate ($m \sim 1$)

$V_T = V_{T0} - \delta V_{DS}$

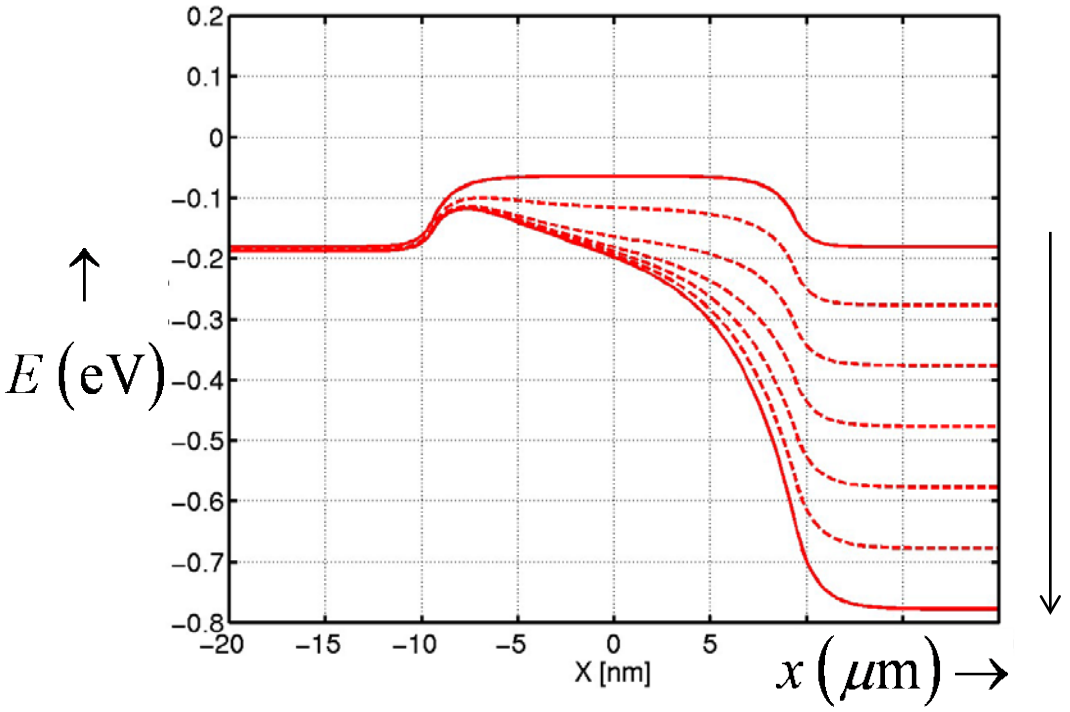
$m = \text{constant}$



3) Additional increases in V_{DS} beyond V_{DSAT} drop near the drain and have a **small effect** on I_{DS} (small DIBL)

"Well-tempered MOSFET"

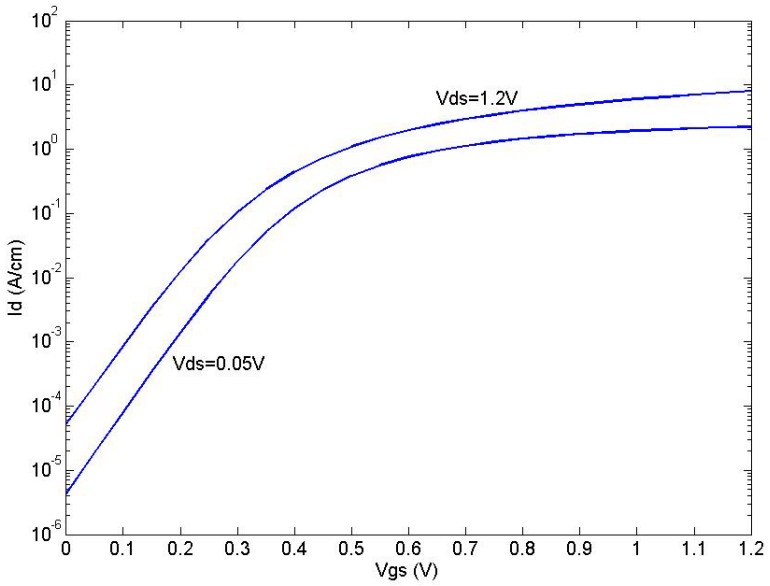
E_X *vs.* *x* for V_{GS} = 0.5V



(Numerical simulations of an *L* = 10 nm double gate Si MOSFET from J.-H. Rhew and M.S. Lundstrom, *Solid-State Electron.,* **46**, 1899, 2002.)

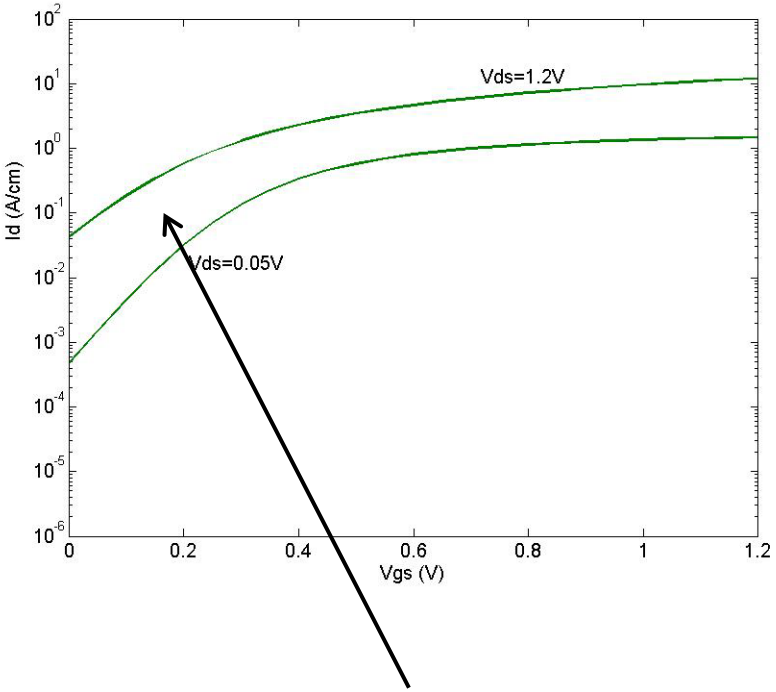
Example

L = 105 nm



(Courtesy, Shuji Ikeda, ATDF, Dec. 2007)

L = 85 nm



Increased DIBL and SS

Summary

2D MOS electrostatics degrade device performance (increases DIBL and SS).

The goal of MOSFET design is to make 1D electrostatics hold at the VS – with small DIBL and a SS parameter, *m*, which is nearly one.

The way to achieve this is to engineer the device such that the gate voltage controls the height of the source to channel energy barrier.

Next Lecture: Let's re-visit the VS model.