Fundamentals of Nanotransistors

Unit 1: Transistor Fundamentals

Lecture1.4: Transistors to Circuits

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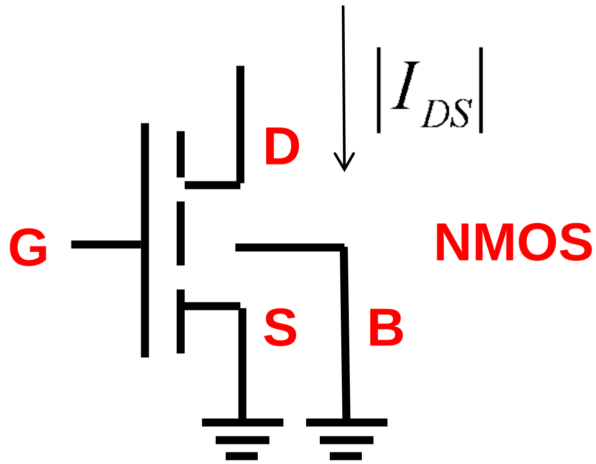
Lecture 1.3 Summary

Given the measured characteristics of a MOSFET, you should be able to determine:

1. on-current: I_{ON}
2. off-current: I_{OFF}
3. subthreshold swing, SS
4. drain induced barrier lowering: DIBL
5. threshold voltage: V_T (lin) and V_T (sat)
6. Drain to source resistance: R_{DS}
7. drain saturation voltage: V_{DSAT}
8. output resistance: r_o
9. *transconductance:* g_m

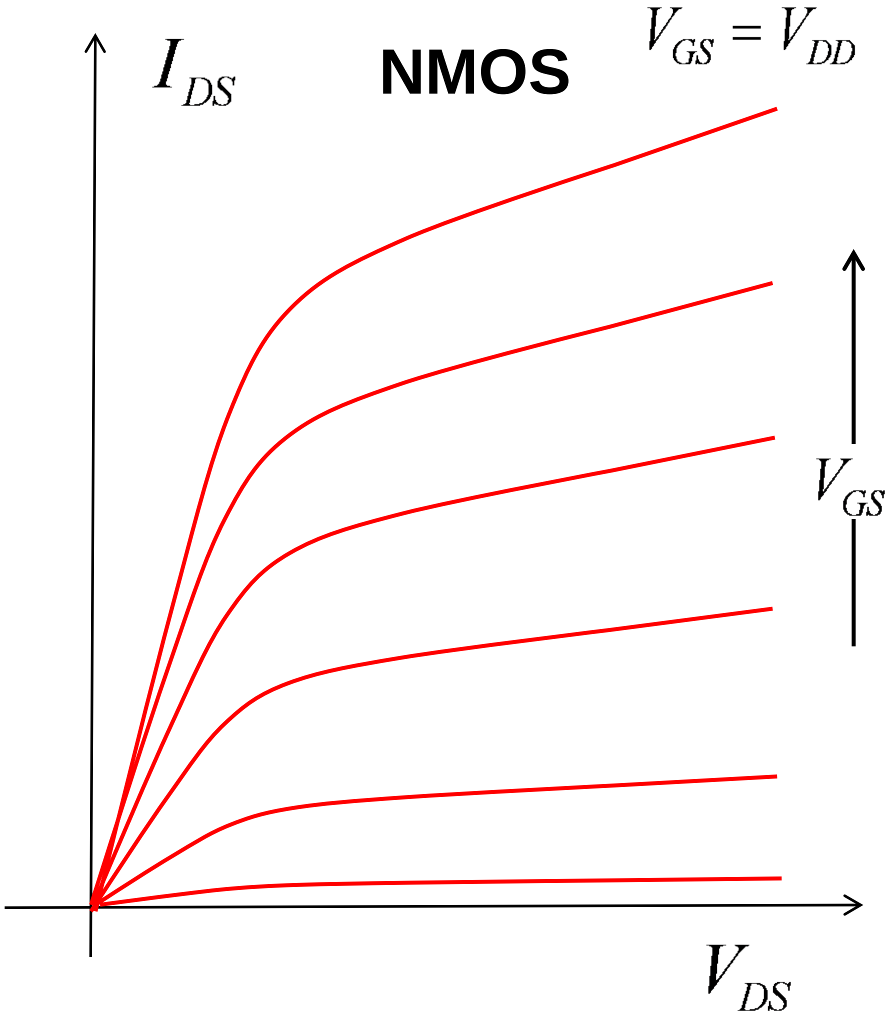
How do these device parameters affect circuit performance?

N-MOSFETs



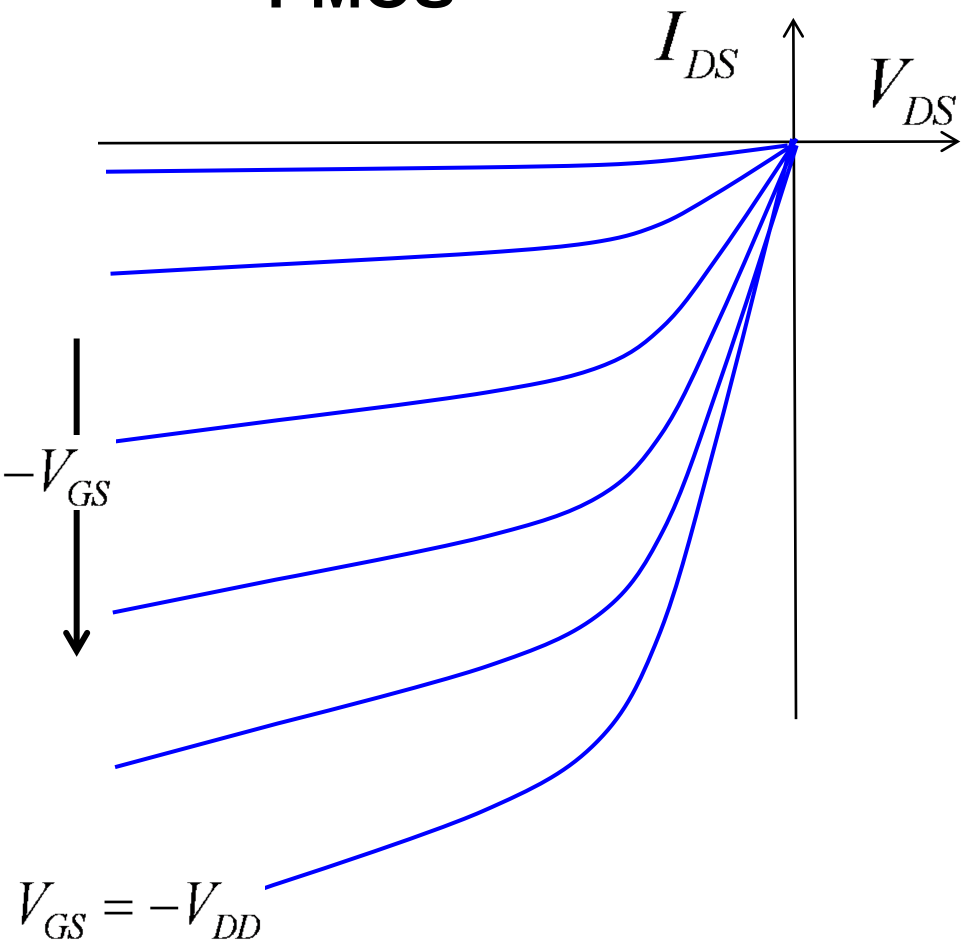
$V_{GS} > V_T \quad V_T > 0$

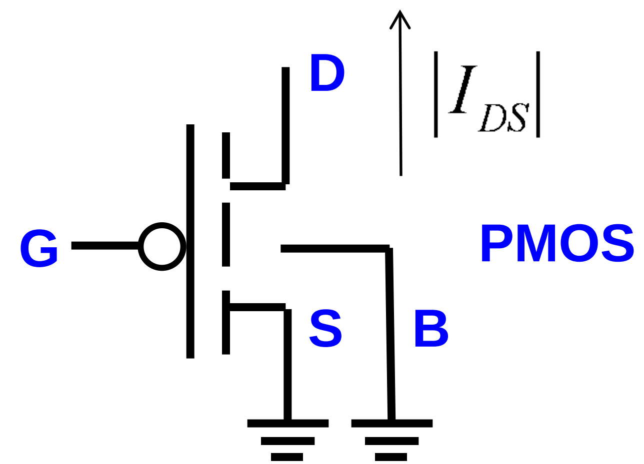
$V_{DS} > 0$



P-MOSFETs

PMOS



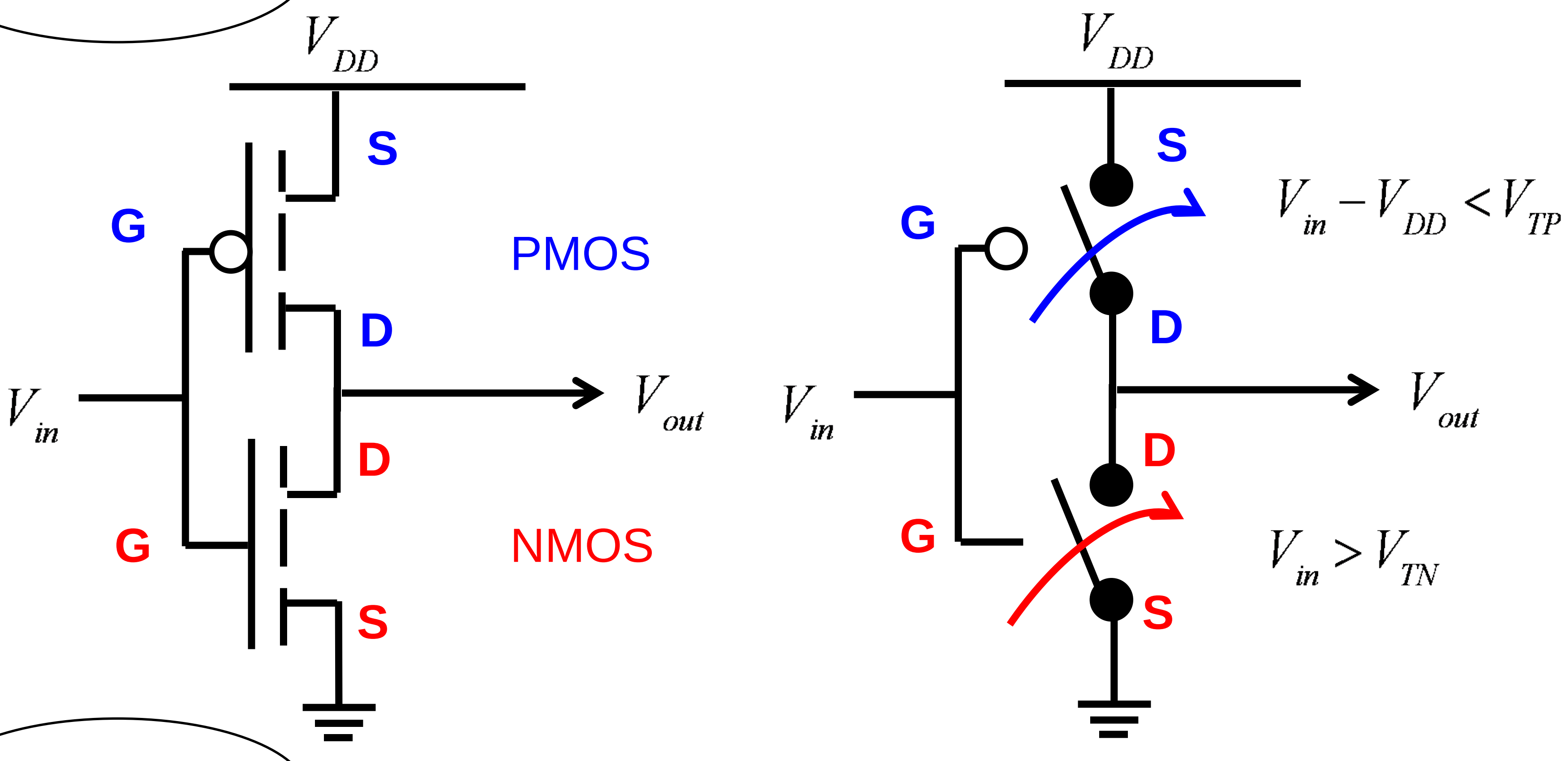


$V_{GS} < V_T \quad V_T < 0$

$V_{DS} < 0$

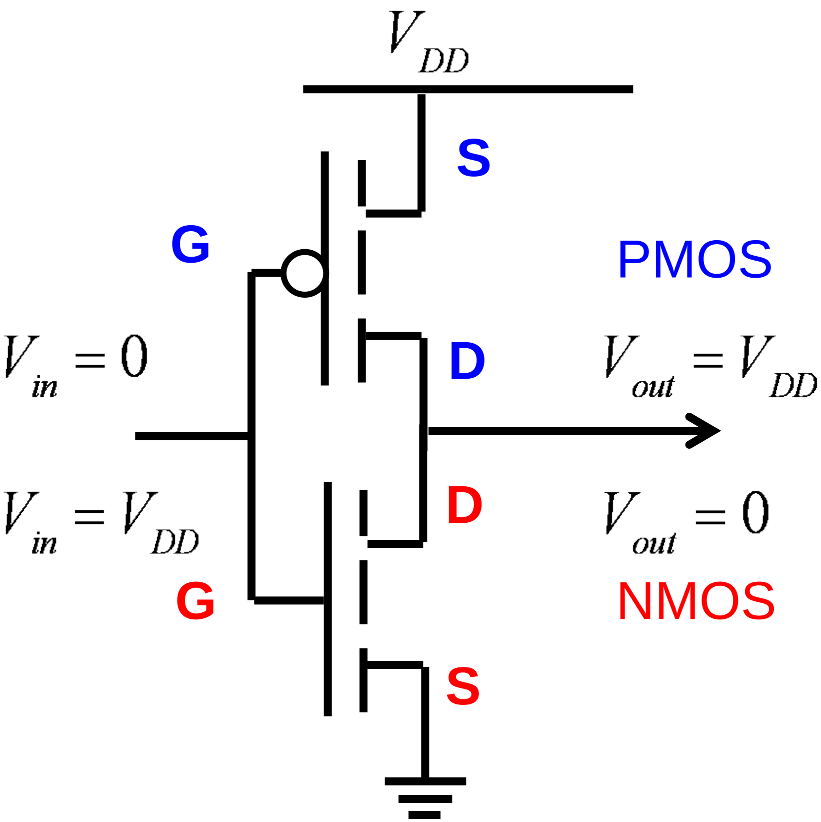
Ideal CMOS inverter

$$V_{GSP} = V_{in} - V_{DD}$$

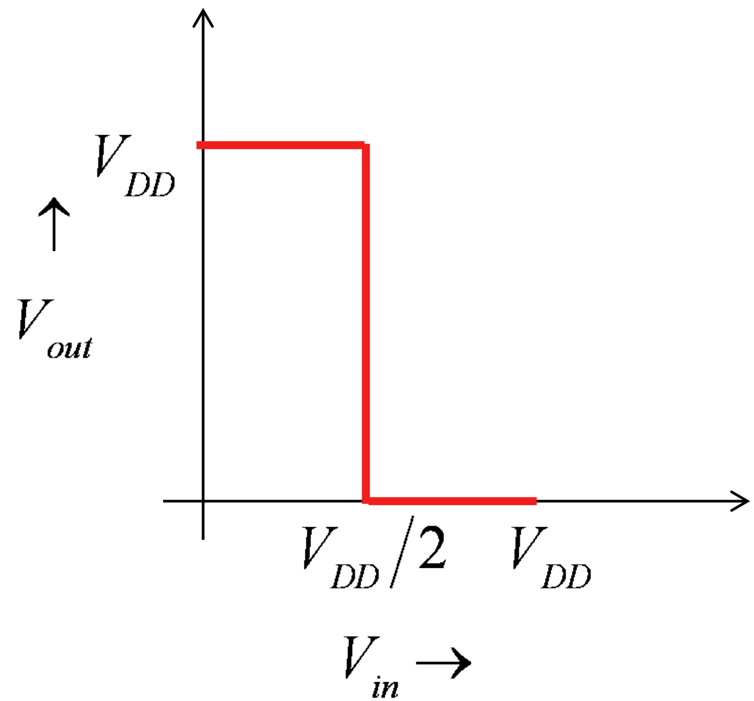


$$V_{GSN} = V_{in}$$

Ideal CMOS inverter



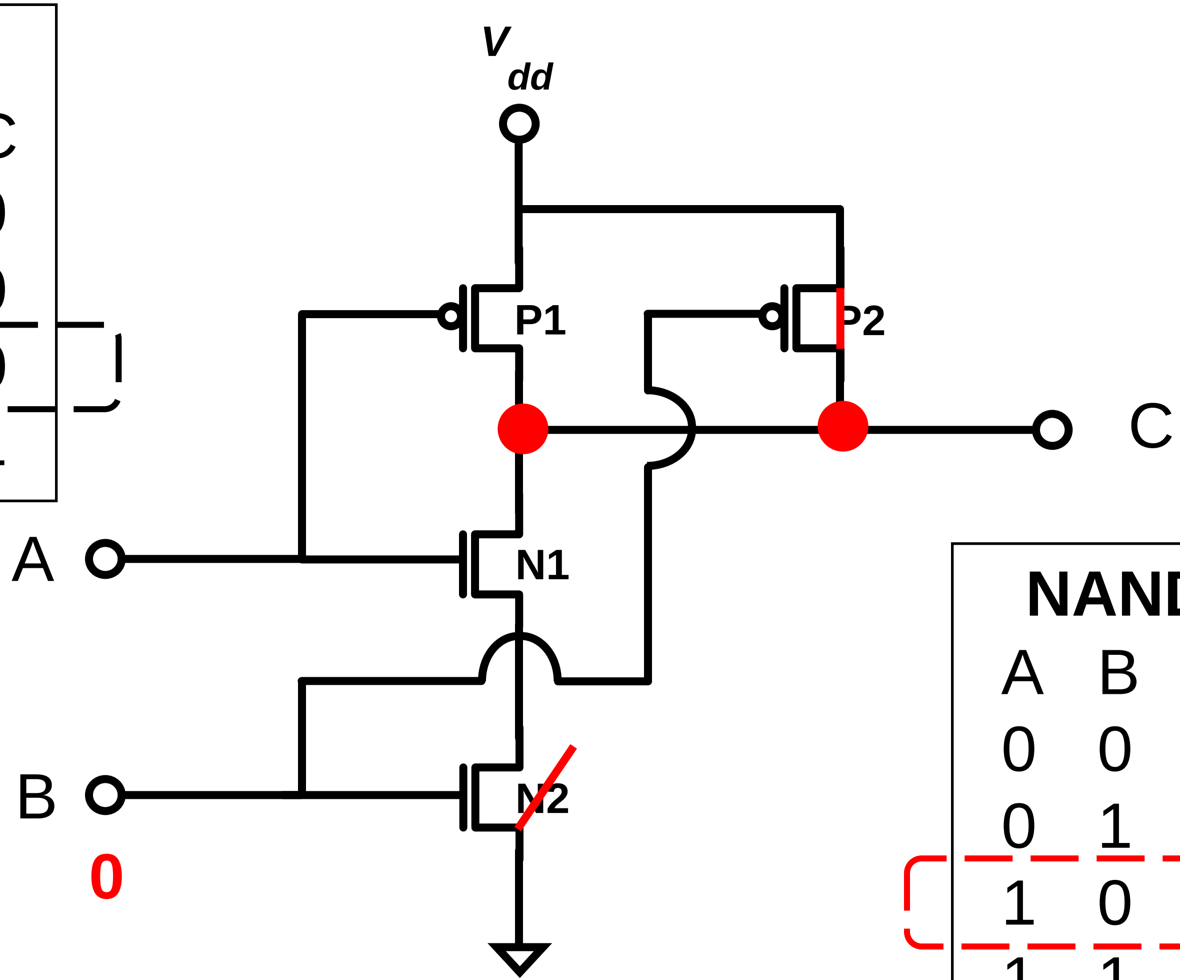
transfer characteristic



2-input NAND gate

AND

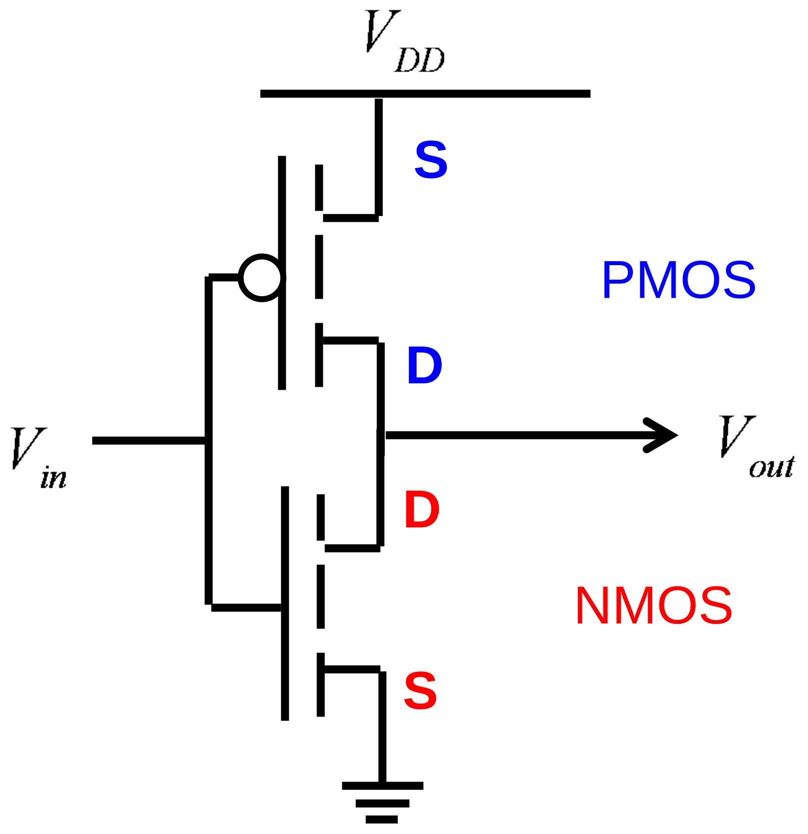
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1



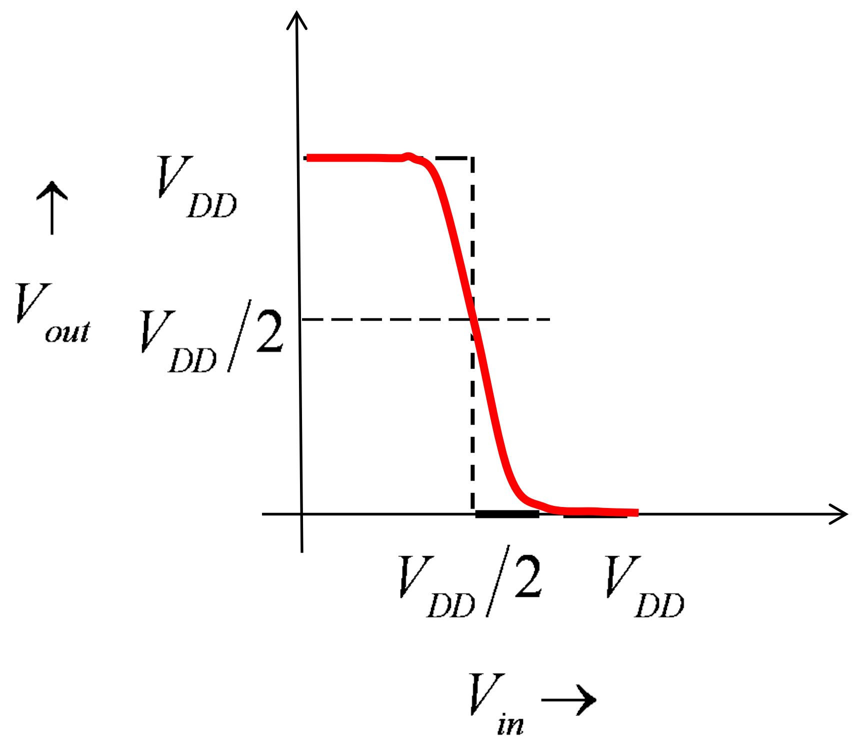
NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

CMOS inverter

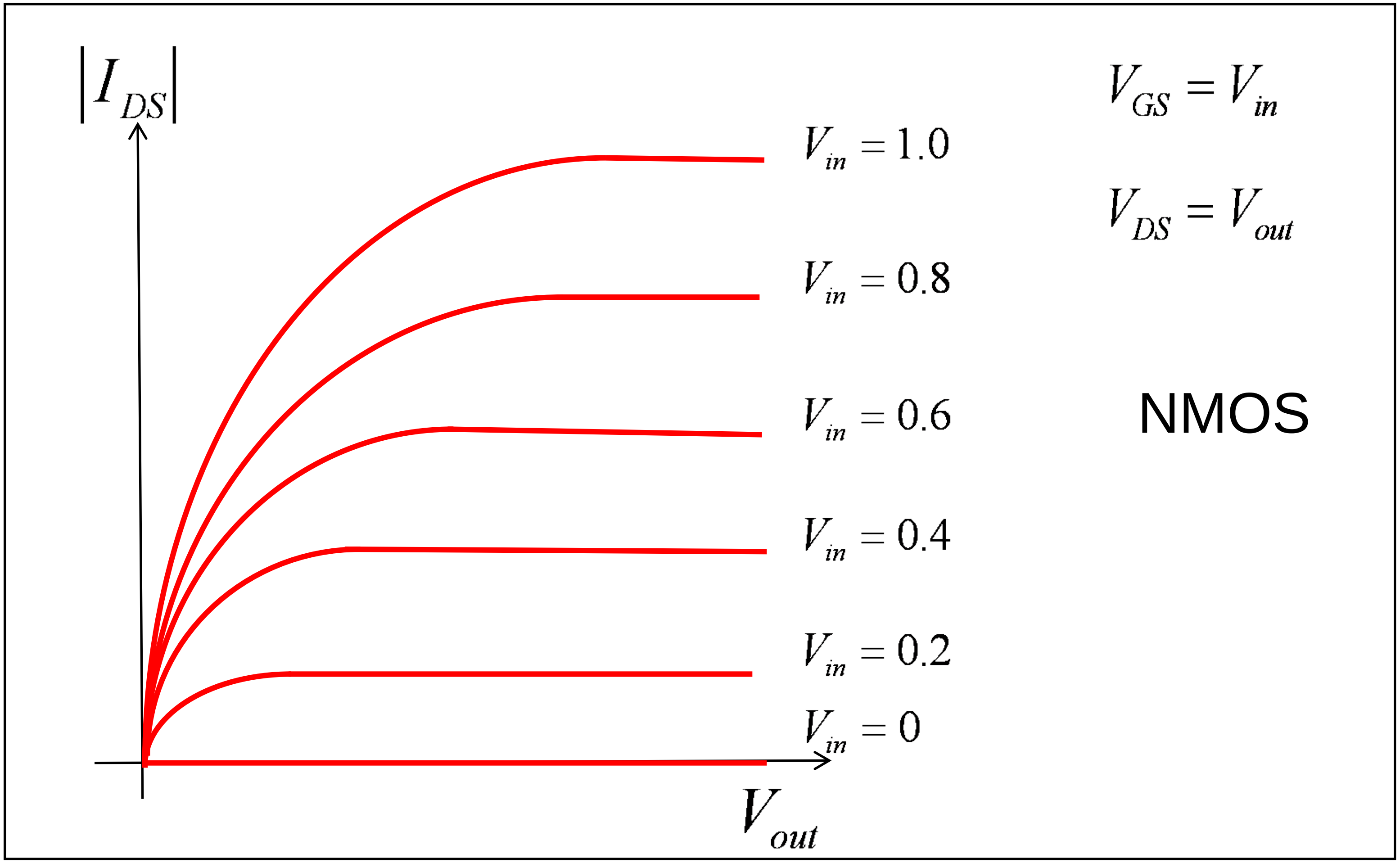


Real transfer characteristic



CMOS inverter: V_{out} vs. V_{in}

$V_{DD} = 1.0\ \text{V}$ $\qquad$ $V_{TN} = -V_{TP} = 0.15\ \text{V}$



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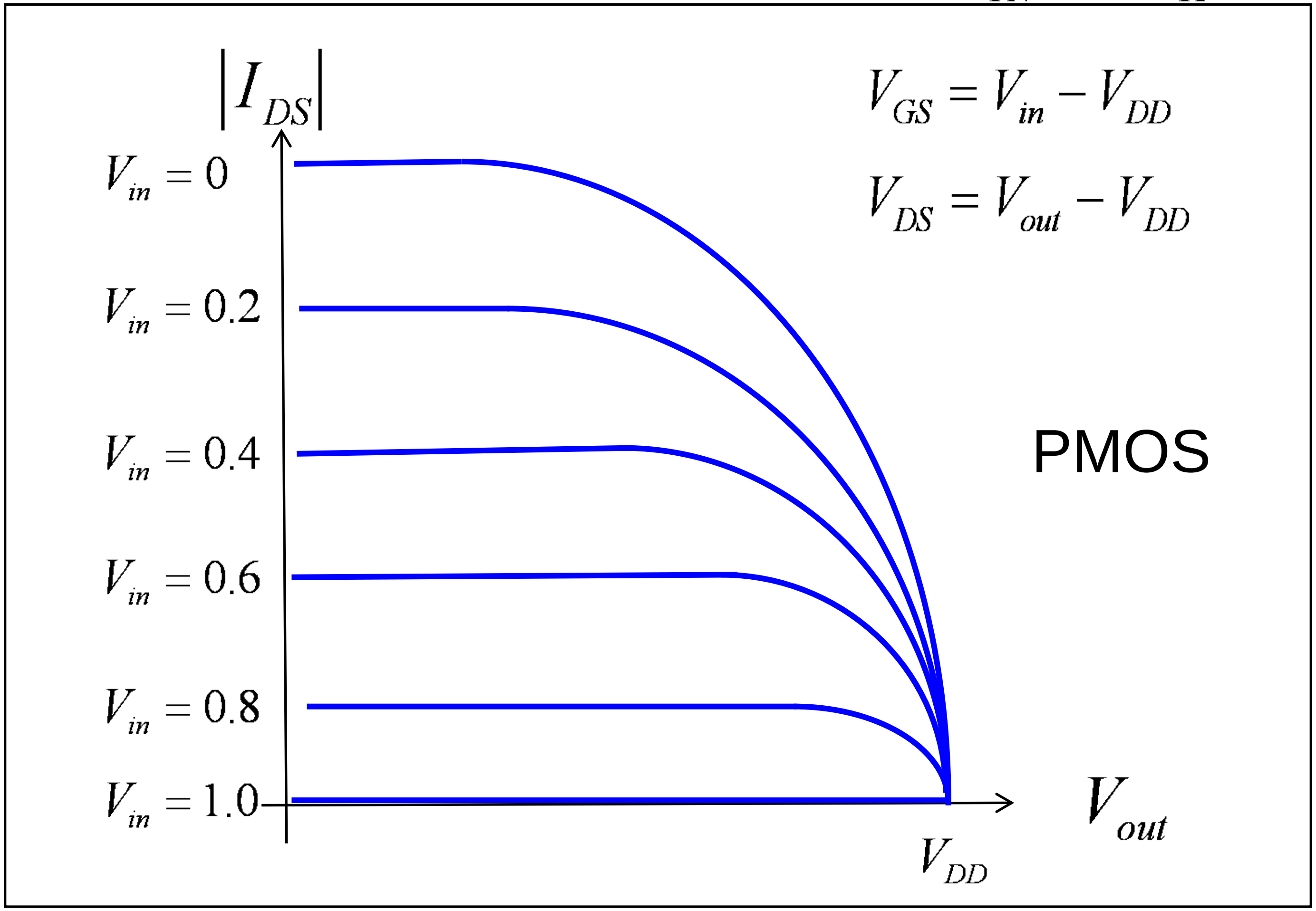

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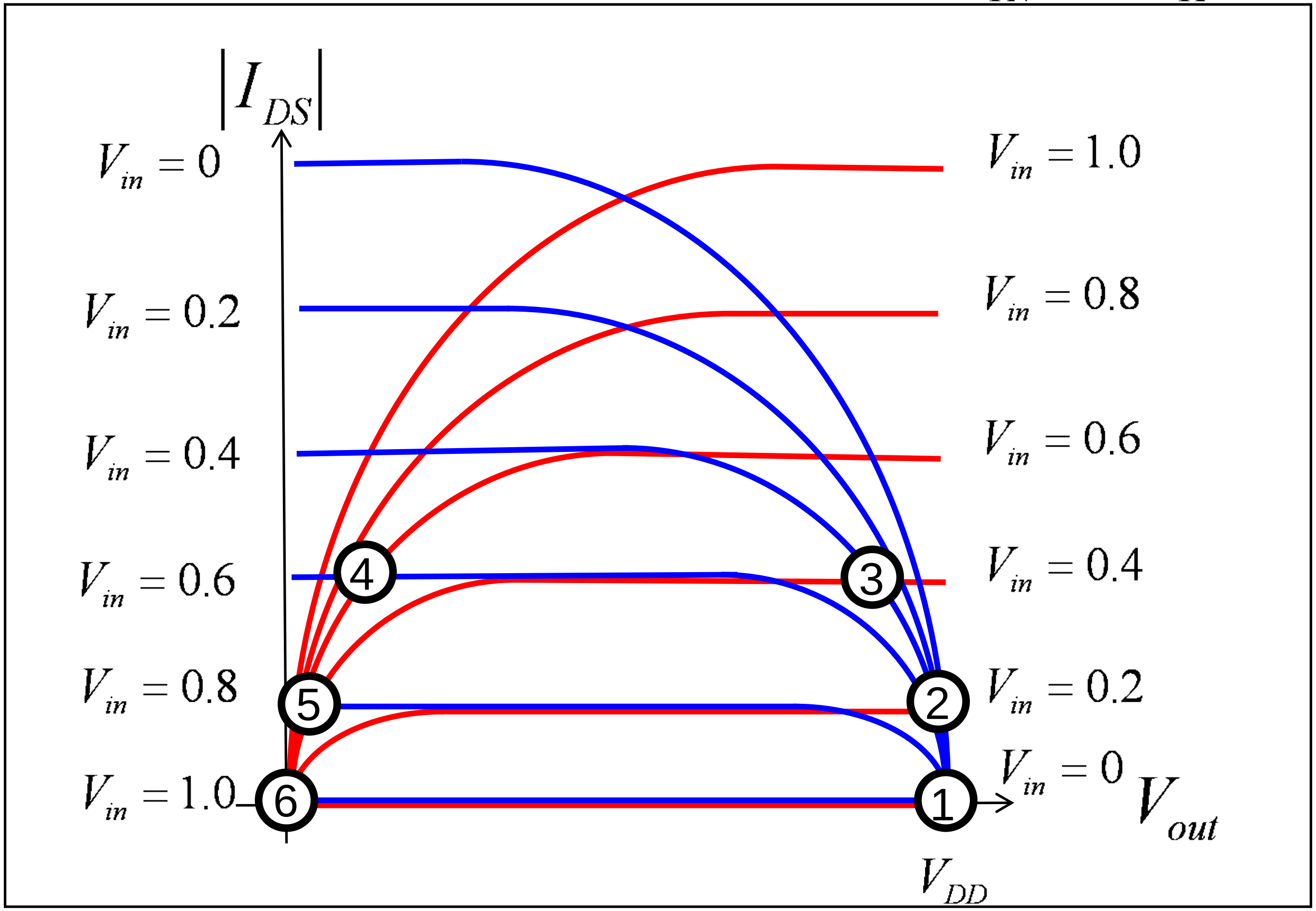
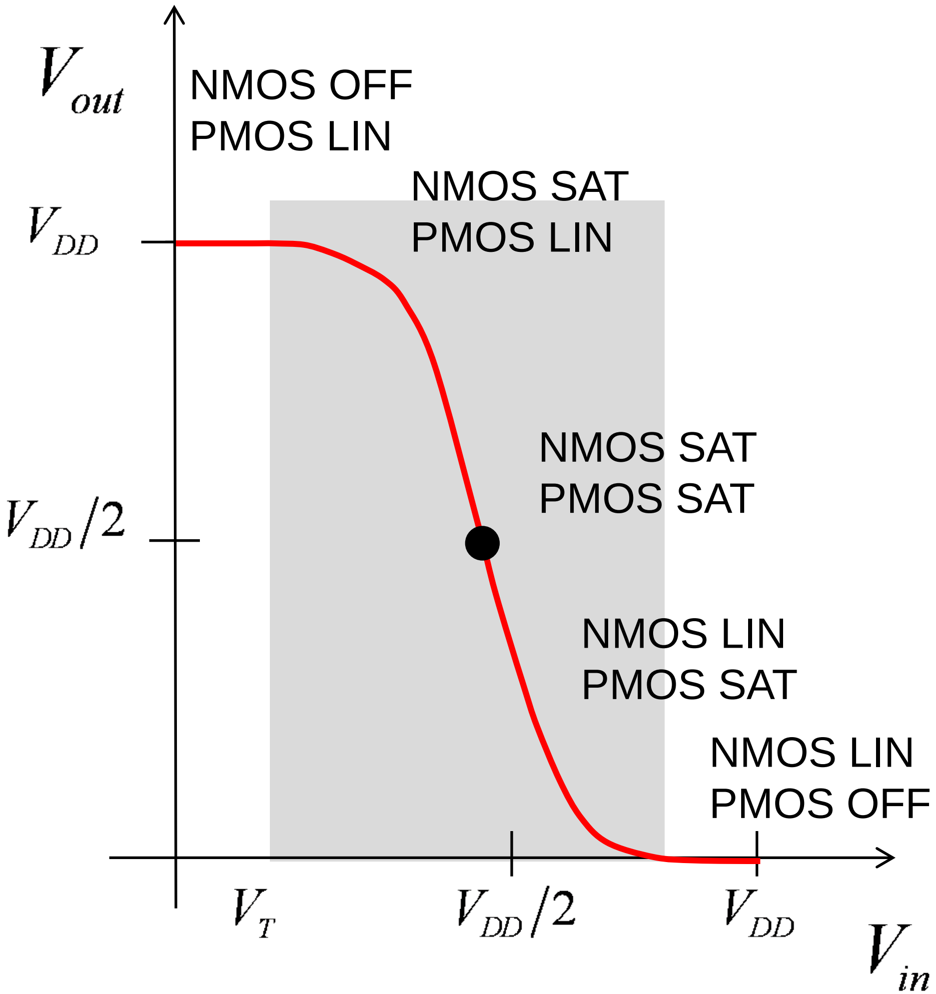


CMOS inverter: current



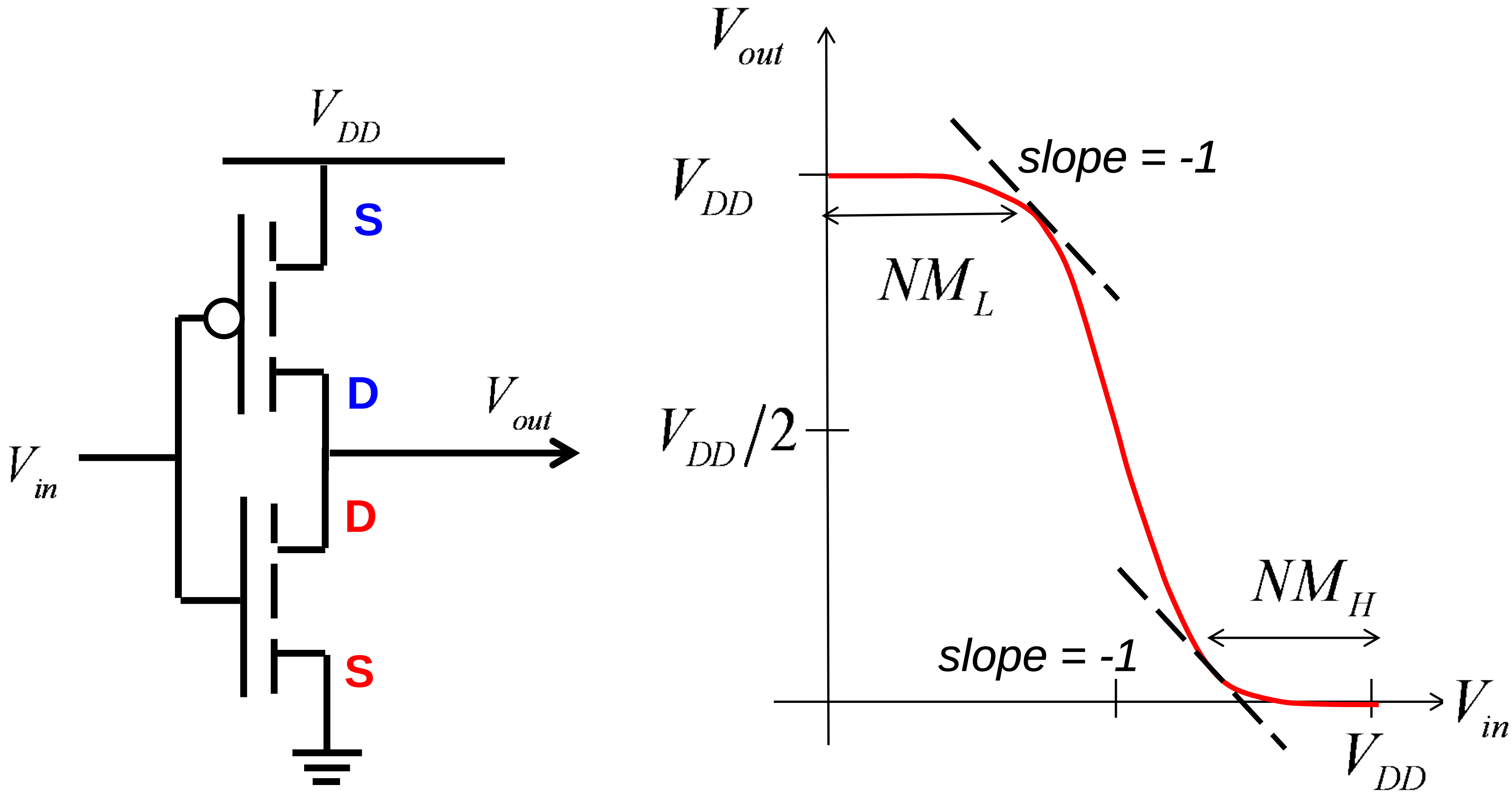
V_{in} = 0: No current flows!

V_{in} = 1: No current flows!

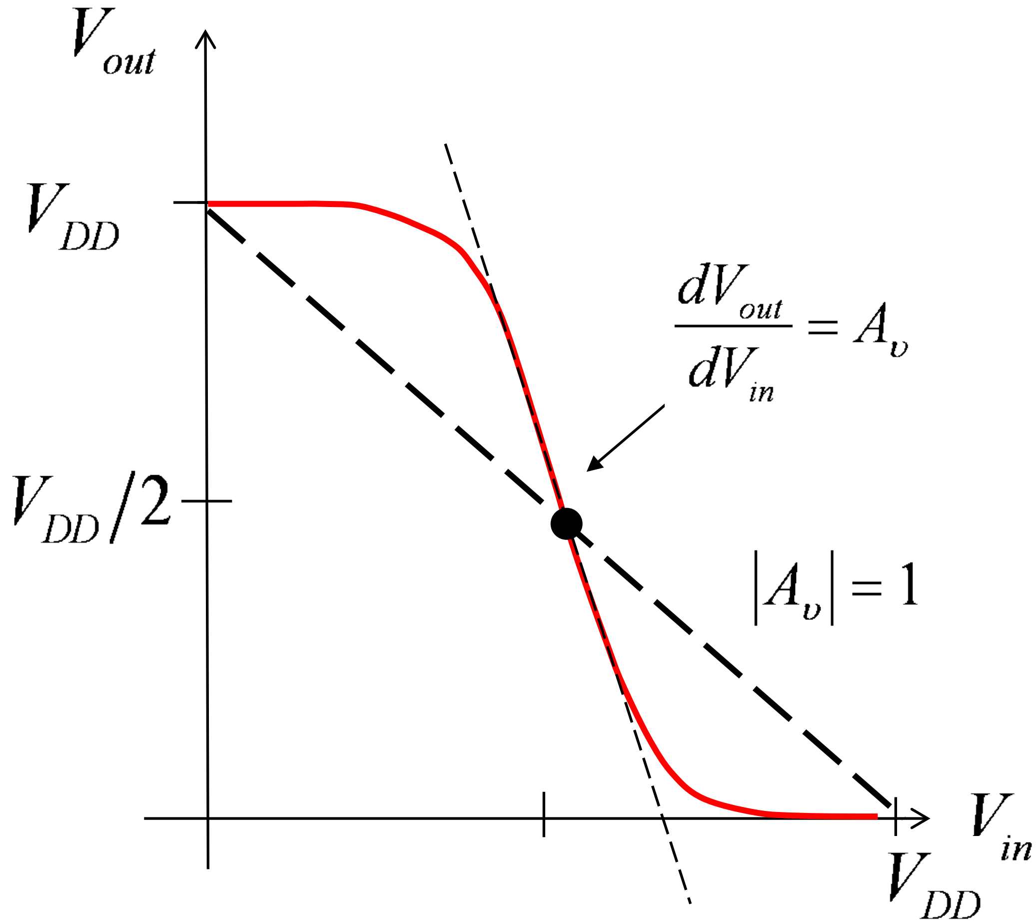
No static power dissipation!

In practice: Little power dissipation when I_{OFF} is small!

CMOS inverter: noise margins



Importance of gain



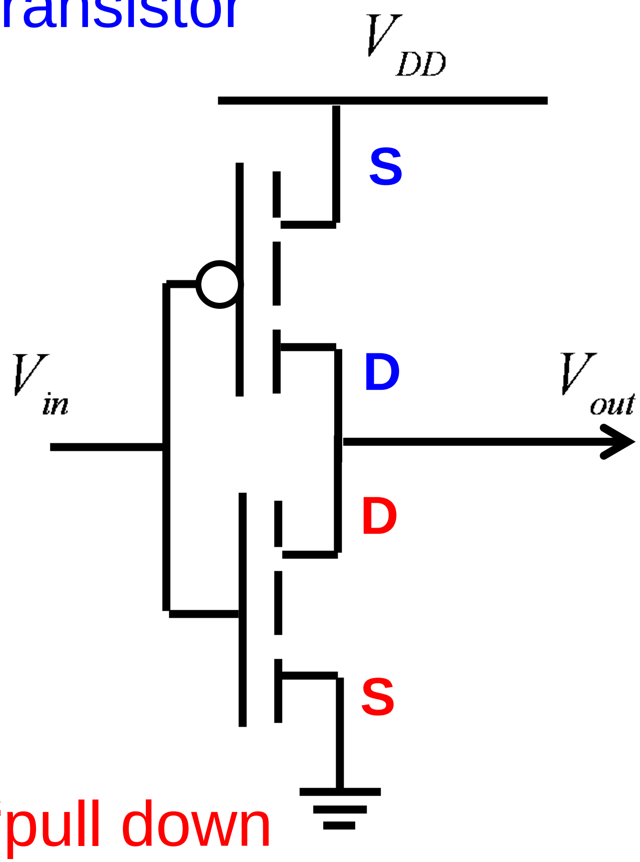
Must have gain to have noise margins

$$\frac{dV_{out}}{dV_{in}} = \frac{dV_{out}}{dI_{DS}} \frac{dI_{DS}}{dV_{in}} = r_0 g_m$$

Must have adequate $g_m r_o$.

CMOS inverter: summary

“pull up transistor”



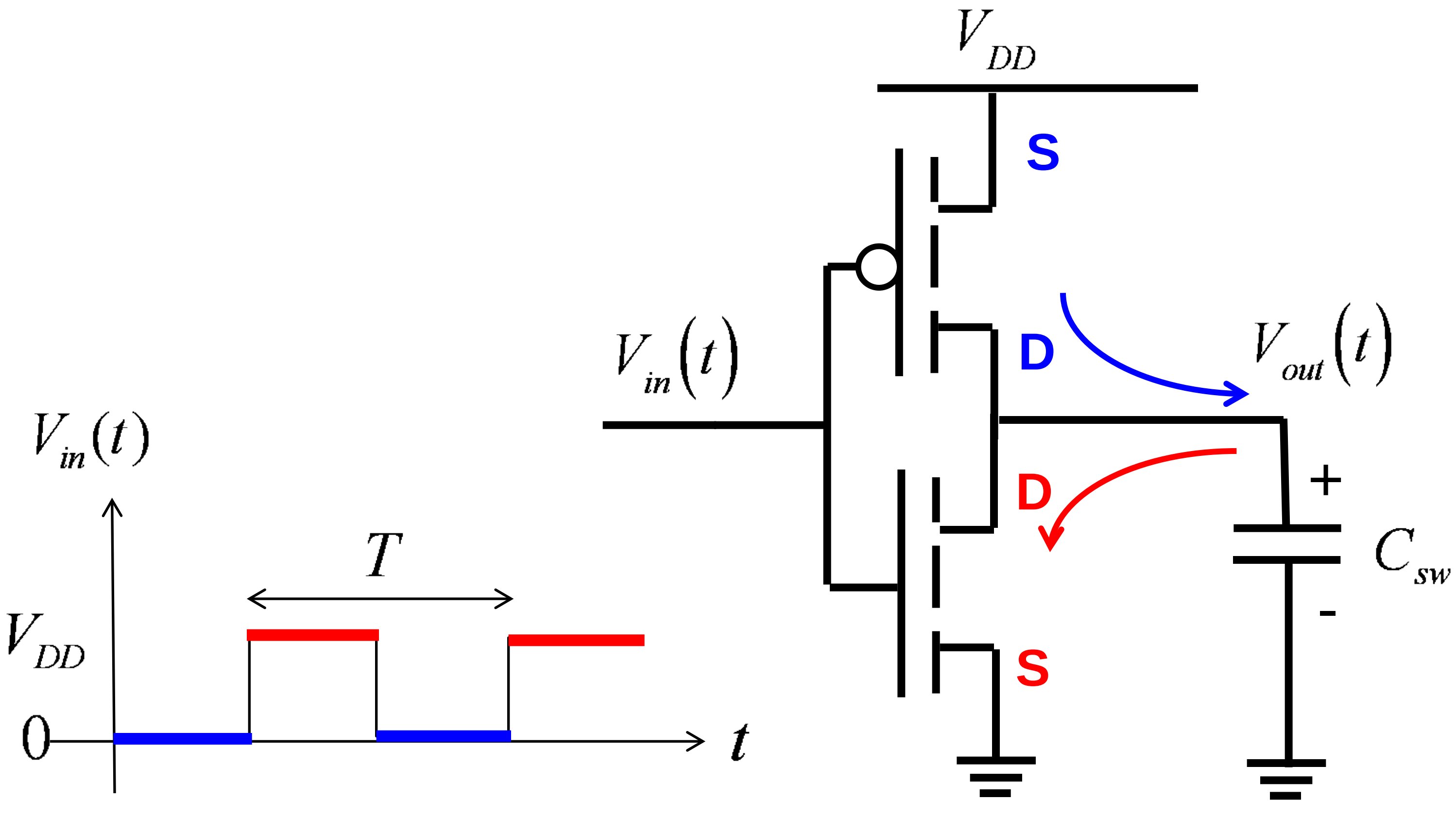
“pull down transistor”

1) Little current flow unless switching. (small power dissipation - **low I_{off}**).

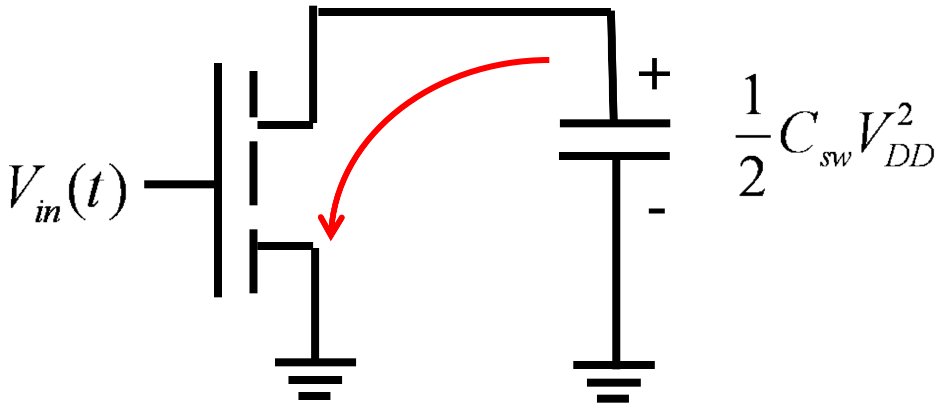
2) Good noise margins if device has high gain (**adequate $g_m r_o$**).

Next: *understand speed and power.*

Dynamic performance



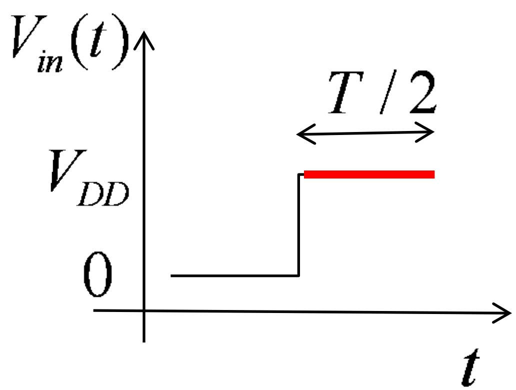
Power dissipation



$$E_C(0) = \frac{1}{2}C_{sw}V_{DD}^2$$

$$E_C(T/2) = 0$$

$$P_{dynamic} = \frac{\Delta E}{T/2} = \frac{C_{sw}V_{DD}^2}{T}$$

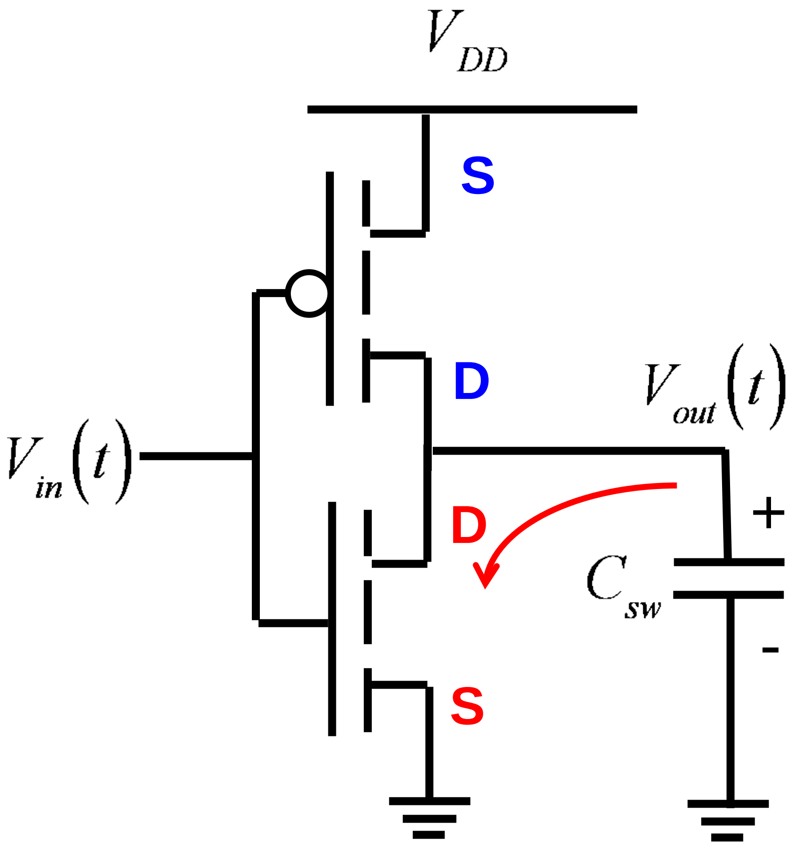


"activity factor"

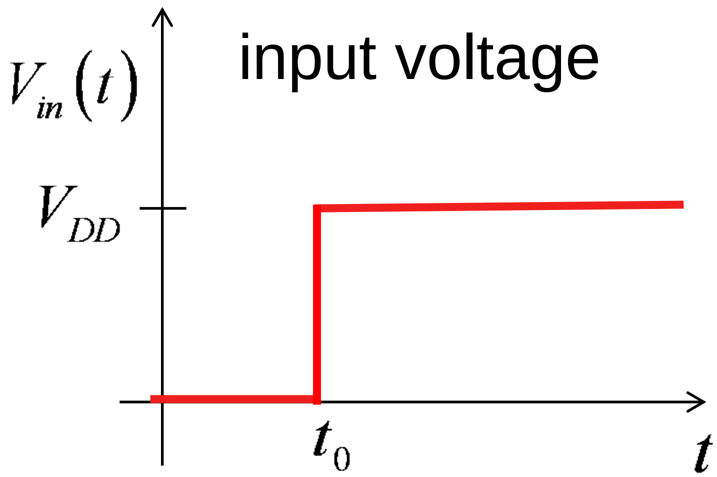
$$P_{dynamic} = \alpha f C_{sw} V_{DD}^2$$

Low power requires low voltage!

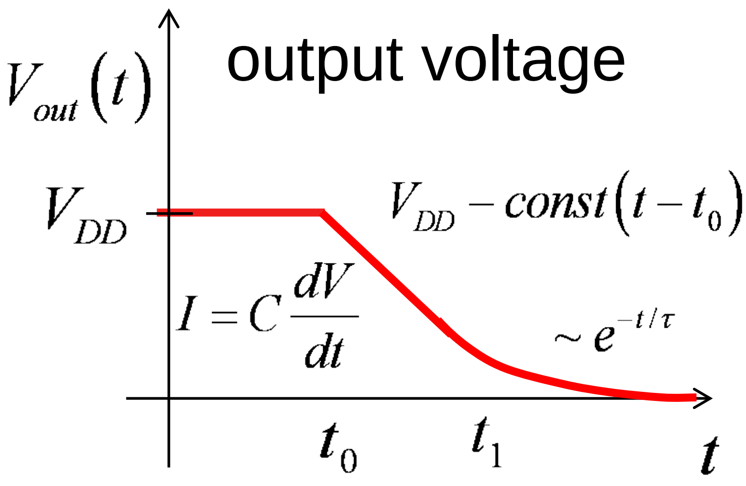
Speed



V_{DD}
S
D
$V_{out}(t)$
$V_{in}(t)$
D
+
C_{sw}
-
S

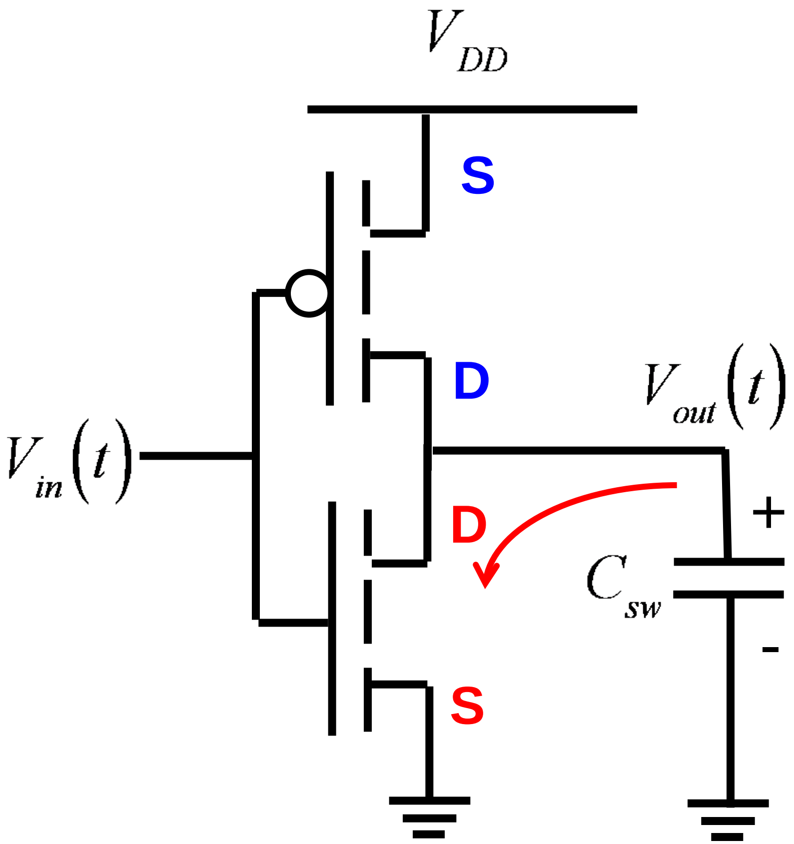


$V_{in}(t)$
input voltage
V_{DD}
t_0
t



$V_{out}(t)$
output voltage
V_{DD}
$V_{DD} - const(t - t_0)$
$I = C\frac{dV}{dt}$
$\sim e^{-t/\tau}$
t_0
t_1
t

Speed



$$I = C\frac{dV}{dt}$$

$$I_{ON} = C_{SW}\frac{\Delta V}{\Delta t} = C_{SW}\frac{V_{DD}/2}{\tau}$$

$$\tau = \frac{1}{2}\frac{C_{sw}V_{DD}}{I_{ON}}$$

Speed is determined by the on-current!

Circuit performance

1) Switching energy: $$E_S = \frac{1}{2} C_{sw} V_{DD}^2$$

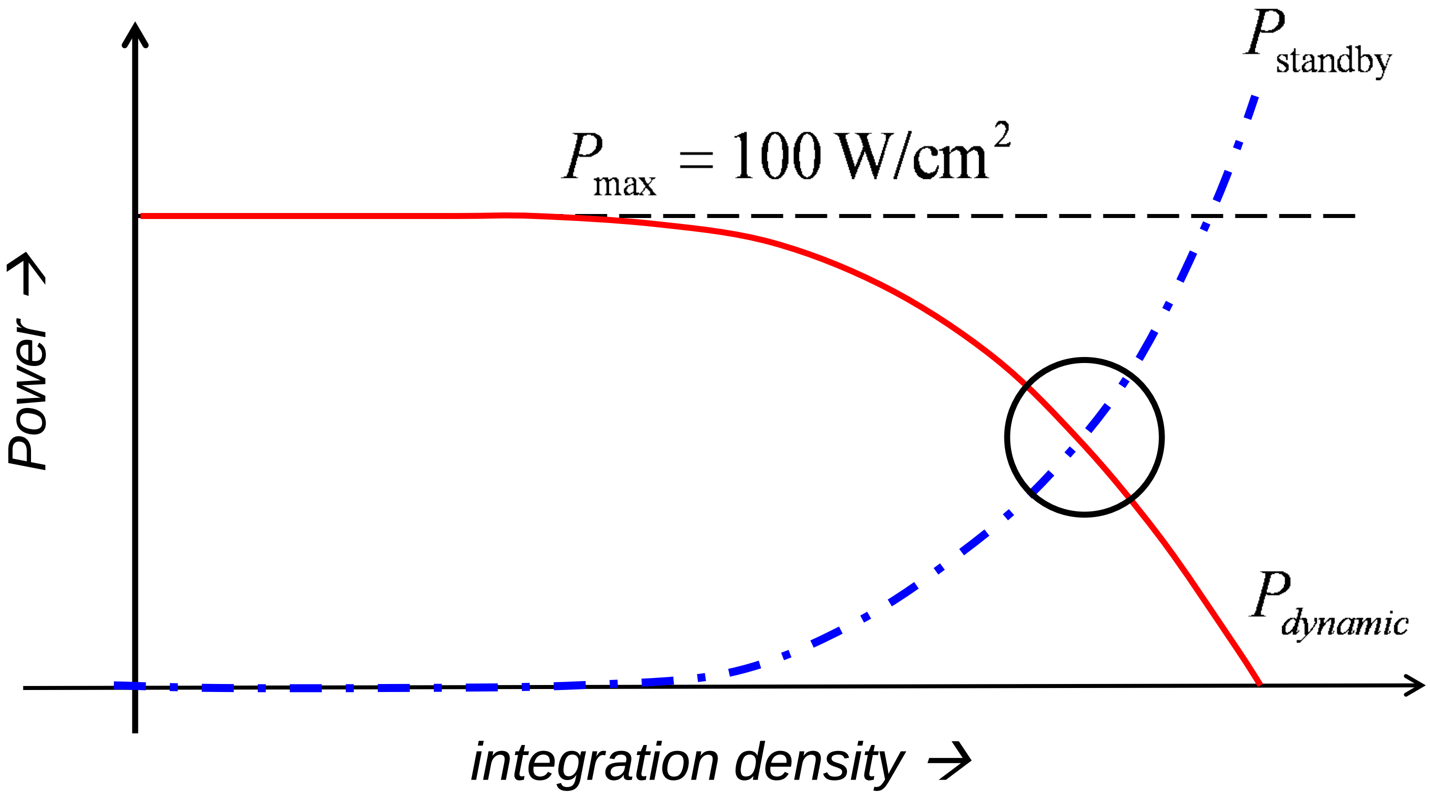
2) Dynamic power: $$P_D = \alpha f C_{sw} V_{DD}^2$$

3) Standby power: $$P_{SB} = I_{OFF} V_{DD}$$

4) Switching delay: $$\tau = \frac{C_{sw} V_{DD}}{2 I_{ON}}$$

5) Noise margins: $$|A_v| = g_m r_0 > 1$$

Power constrained design



(Dave Frank, IBM)

Summary

Now that we understand a little bit about how circuit performance is related to key device metrics, we will focus for the rest of the course on how nanoscale transistors work.

Next topic: A simple (energy band) view of how MOSFETs work.