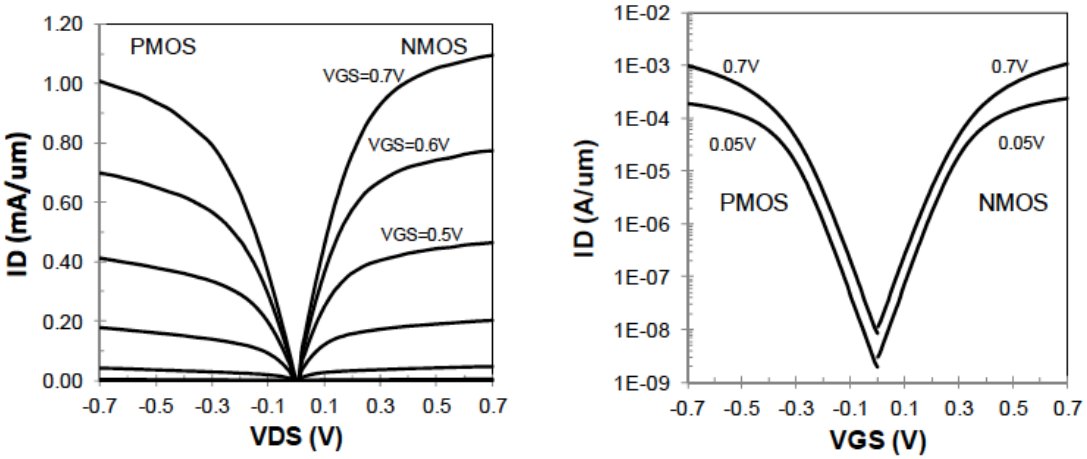
Fundamentals of Nanotransistors
Unit 1 Homework SOLUTIONS

Mark Lundstrom
Purdue University
November 2, 2015
(Revised Feb. 3, 2016)

1) The *IV* characteristics of an N-MOSFET for the 14 nm technology node are shown below. Reading from the graphs as carefully as you can, estimate the following key device metrics and other parameters for this device.

   a) threshold voltage assuming that the device is "on" when $I_D = 10^{-5}$ A/μm.
   b) on-current: I_{ON}
   c) off-current: I_{OFF}
   d) subthreshold swing, SS
   e) drain induced barrier lowering: DIBL
   f) total drain to source resistance: R_{TOT} (in the linear region for V_{GS} = 0.7 V)
   g) drain saturation voltage: V_{DSAT} (for V_{GS} = 0.7 V)
   h) output resistance: r_o (in the saturation region for V_{GS} = 0.7 V)
   i) transconductance: g_m (for V_{GS} = 0.7 V, V_{DS} = 0.7 V)

   Be sure to include units for all of your answers.



Source:
S. Natarajan, et al., "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 um2 SRAM cell size," pp. 70-72. Tech. Digest, Intern. Electron Dev. Mtg, Dec. 2014.

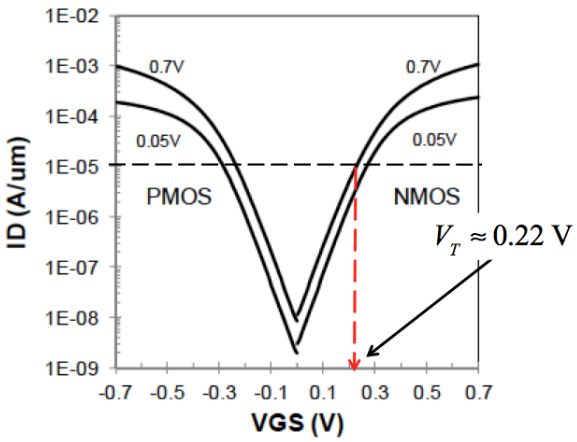
1) Solution

The figures below show how to pull these numbers off of the plots. The emphasis is on the procedure, not on precise, numerical values.

Unit 1 Homework SOLUTIONS (continued)

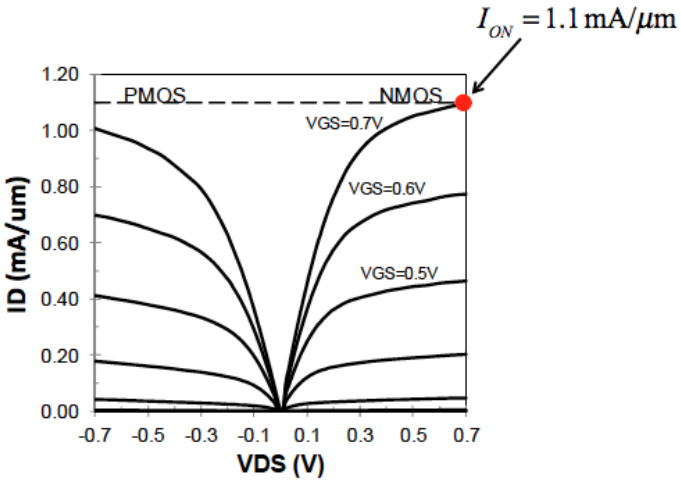
1a) Threshold voltage:

Note that "threshold voltage" is an imprecisely defined quantity because the transition from off to on is smooth and continuous. There are many ways to extract a threshold voltage and each one gives a little different answer. We use here a very simple, but widely-used, approach.



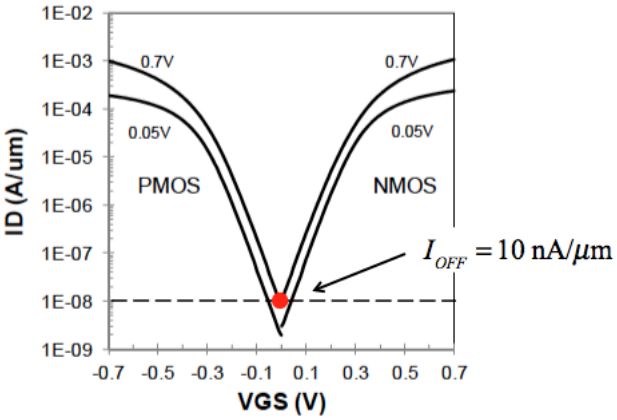
Note that if we had used the $V_{DS} = 0.05$V curve, we would have deduced a slightly larger threshold voltage, which is an indication of DIBL.

1b) On-current:

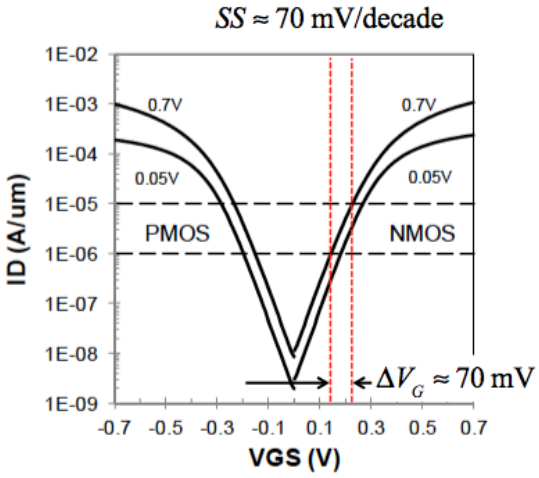


Unit 1 Homework SOLUTIONS (continued)

1c) Off-current:

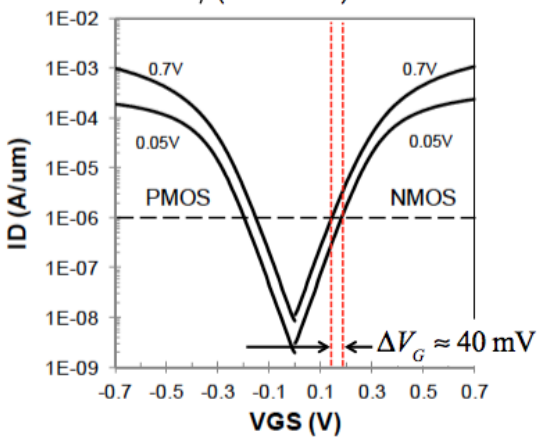


1d) Subthreshold swing:



1e) Drain-induced barrier lowering:

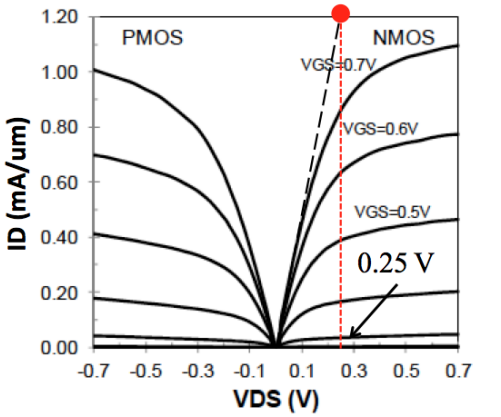
$$DIBL \approx 40/(0.7-0.05) \approx 62 \text{ mV/V}$$



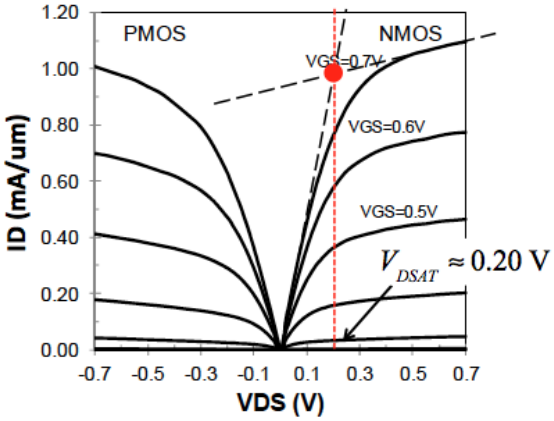
Unit 1 Homework SOLUTIONS (continued)

1f) Total drain to source resistance in the liner region:

$$R_{TOT} = 0.25 \text{ V} / (1.2 \text{ mA}/\mu\text{m}) \approx 200\ \Omega - \mu\text{m}$$

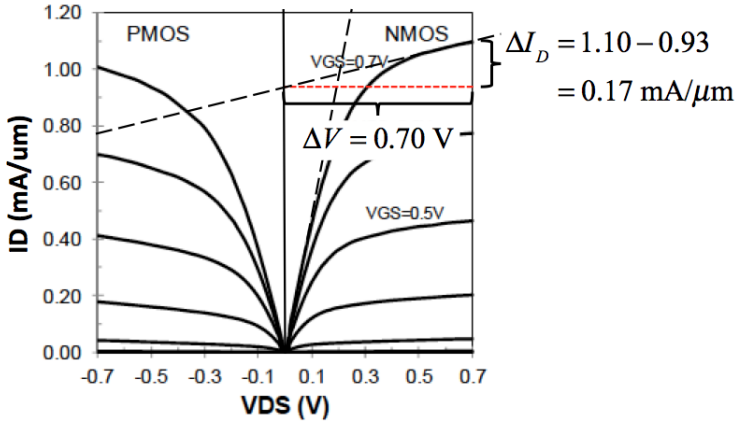


1g) Drain saturation voltage for V_{GS} = 0.7 V.



1h) Output resistance:

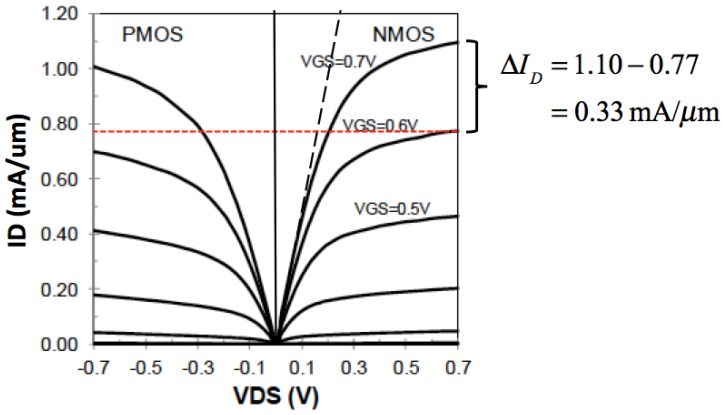
$$r_0 = 0.70\text{ V} / \left(0.17\text{ mA}/\mu\text{m}\right) \approx 4100\ \Omega\text{-}\mu\text{m}$$



Unit 1 Homework SOLUTIONS (continued)

1h) Transconductance:

$$g_m \approx \left(0.33\text{ mA}/\mu\text{m}\right)/0.10\text{ V} \approx 3.3\text{ mS}/\mu\text{m}$$



Summary of results:

a) threshold voltage, V_T, at $I_D = 10^{-5}$ A/μm	$V_T = 0.22$ V
b) on-current, I_{ON}	$I_{ON} = 1.1$ mA/μm
c) off-current, I_{OFF}	$I_{OFF} = 10$ nA/μm
d) subthreshold swing, SS	$SS \approx 70$ mV/decade
e) drain induced barrier lowering: $DIBL$	$DIBL \approx 62$ mV/V
f) total drain-source resistance: R_{TOT} (linear reg. V_{GS} = 0.7 V)	$R_{TOT} \approx 200\ \Omega - \mu$m
g) drain saturation voltage, V_{DSAT} (for V_{GS} = 0.7 V)	$V_{DSAT} \approx 0.20$ V

h) output resistance, r_o (in the saturation region for V_{GS} = 0.7 V) $r_0 \approx 4100\,\Omega\text{-}\mu\text{m}$

i) transconductance, g_m (for V_{GS} = 0.7 V, V_{DS} = 0.7 V)

$$g_m \approx 3.3\,\text{mS}/\mu\text{m}$$

2) Measured *IV* data for an N-MOSFET are shown below. Relevant parameters for this MOSFET are:

T = 300 K

Oxide thickness: $x_0 = 2.2$ nm Relative dielectric constant: $\kappa_{ox} = 4$

Power supply voltage: $V_{DD} = 1.2$ V Series resistances: $R_{S0} = R_{D0} = 80\,\Omega - \mu\text{m}$

Channel length = 85 nm Channel width, $W = 10^{-4}$ cm.

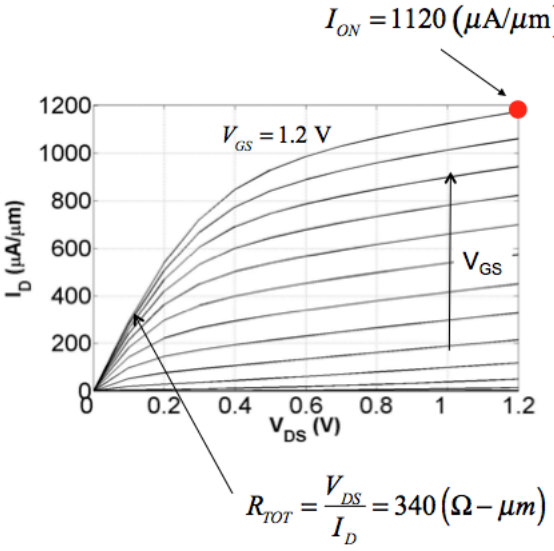
$V_{TLIN} = 0.28$ V.

Unit 1 Homework SOLUTIONS (continued)

Answer the following questions.

2a) What is the resistance of the intrinsic channel for $V_{GS} = 1.2$ V?

2b) Estimate the mobility of electrons in the channel at $V_{GS} = 1.2$ V?



Solutions:

2a) What is the resistance of the intrinsic channel for $V_{GS} = 1.2$ V?

The total resistance between the source and drain is:

$R_{TOT} = R_{CH} + R_{S0} + R_{D0} = 340 \quad \Omega\text{-}\mu\text{m}$

So the channel resistance is:

$$R_{CH} = R_{TOT} - R_{S0} - R_{D0} = 340 - 80 - 80 = 180 \quad \Omega\text{-}\mu\text{m}$$

$$\boxed{R_{CH} = 180 \quad \Omega\text{-}\mu\text{m}}$$

2b) Estimate the mobility of electrons in the channel at $V_{GS} = 1.2$ V?

$$I_{DLIN} = \frac{W}{L}\mu_n C_{ox}\left(V_{GS} - V_{TLIN}\right)V_{DS} = V_{DS}/R_{CH}$$

$$R_{CH} = \frac{1}{\mu_n C_{ox}\left(V_{GS} - V_{TLIN}\right)}\frac{L}{W}$$

$$\mu_n = \frac{1}{R_{CH} C_{ox}\left(V_{GS} - V_{TLIN}\right)}\frac{L}{W}$$

$$C_{ox} = \frac{K_0\varepsilon_0}{x_0} = \frac{4 \times 8.854 \times 10^{-14} \text{ F/cm}}{2.2 \times 10^{-7} \text{ cm}} = 1.61 \times 10^{-6} \text{ F/cm}^2$$

Unit 1 Homework SOLUTIONS (continued)

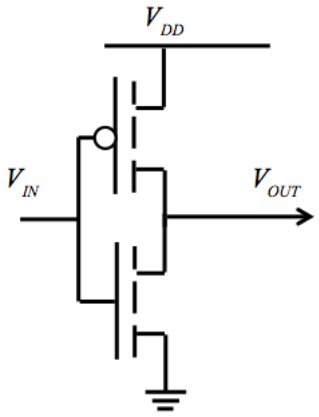
The width is given as one micrometer.

$$\mu_n = \frac{1}{180 \times 1.61 \times 10^{-6}\left(1.2 - 0.28\right)}\frac{85}{1000} = 320 \text{ cm}^2/\text{V-s}$$

$$\boxed{\mu_n = 320 \text{ cm}^2/\text{V-s}}$$

Note that we have not accounted for the voltage drop across the source series resistance. The internal gate to source voltage is a little smaller that the 1.2 V assumed here. There are many papers on how to accurately extract the mobility from measured IV characteristics. The calculation here should be viewed as an approximate way to get close to the real answer.

3) A CMOS inverter is shown below. Assume that the NMOS and PMOS transistors in this circuit are the same ones shown in problem 1). Assume that $V_{DD} = 0.7$ V. For each of the input voltages list below, determine the region of operation for each of the transistors.
   a) $V_{IN} = 0.0$ V
   b) $V_{IN} = 0.15$V
   c) $V_{IN} = 0.35$ V
   d) $V_{IN} = 0.70$ V



Solution:

From problem 1), $V_{TN} \approx 0.22$ V and $V_{TP} \approx -0.22$ V.

Also recall from problem 1) that $V_{DSAT}\Big)_N \approx 0.2$ V for high gate voltage. Let's assume that $V_{DSAT}\Big)_P \approx -0.2$ V.

Now examine each of the four cases.

Unit 1 Homework SOLUTIONS (continued)

3a) $V_{IN} = 0.0$ V

$V_{GS}\Big)_N = V_{IN} - 0 = 0 \text{ V} < V_{TN}$ (NMOS is OFF)

$V_{GS}\Big)_P = V_{IN} - V_{DD} = -0.7 \text{ V} < V_{TP}$ (PMOS is ON)

Since the PMOS is ON and the NMOS OFF, the output node is connected to V_{DD} so, $V_{OUT} = 0.7$.

$V_{DS}\Big)_N = V_{OUT} - 0 = 0.7 \text{ V} > V_{DSAT}\Big)_N$ (NMOS is in SATURATION)

$V_{DS}\Big)_P = V_{OUT} - V_{DD} = 0.7 - 0.7 = 0.0 \text{ V} > V_{DSAT}\Big)_P$ (PMOS is in the LINEAR region)

We can say that the NMOS is CUTOFF or that it is in the SATURATION region in subthreshold.

The PMOS is ON and in the LINEAR region.

3b) $V_{IN} = 0.15$V

Similar considerations apply here.

$V_{GS}\Big)_N = V_{IN} - 0 = 0.15 \text{ V} < V_{TN}$ (NMOS is OFF)

$V_{GS}\big)_P = V_{IN} - V_{DD} = 0.15 - 0.7\ \text{V} = -0.55\ \text{V} < V_{TP}$ (PMOS is ON)

Since the PMOS is still ON and the NMOS is still OFF, the output node is connected to V_{DD} so, $V_{OUT} \approx 0.7$.

$V_{DS}\big)_N = V_{OUT} - 0 \approx 0.7\ \text{V} > V_{DSAT}\big)_N$ (NMOS is in SATURATION)
$V_{DS}\big)_P = V_{OUT} - V_{DD} \approx 0.7 - 0.7 = 0.0\ \text{V} > V_{DSAT}\big)_P$ (PMOS is in the LINEAR region)

We can say that the NMOS is still CUTOFF or that it is in the SATURATION region in subthreshold.

The PMOS is still ON and in the LINEAR region.

3c) $V_{IN} = 0.35\ \text{V}$
$V_{GS}\big)_N = V_{IN} - 0 = 0.35\ \text{V} > V_{TN}$ (NMOS is ON)
$V_{GS}\big)_P = V_{IN} - V_{DD} = 0.35 - 0.7\ \text{V} = -0.35\ \text{V} < V_{TP}$ (PMOS is ON)

Unit 1 Homework SOLUTIONS (continued)

For a properly designed inverter with $V_{IN} = V_{DD}/2$, we expect that
$V_{OUT} = V_{DD}/2 = 0.35\ \text{V}$.
$V_{DS}\big)_N = V_{OUT} - 0 \approx 0.35\ \text{V} > V_{DSAT}\big)_N$ (NMOS is in SATURATION)
$V_{DS}\big)_P = V_{OUT} - V_{DD} \approx 0.35 - 0.7 = -0.35\ \text{V} < V_{DSAT}\big)_P$ (PMOS is in SATURATION)

Both the NMOS and PMOS are ON and in SATURATION.

3d) $V_{IN} = 0.70\ \text{V}$
$V_{GS}\big)_N = V_{IN} - 0 = 0.70\ \text{V} > V_{TN}$ (NMOS is ON)
$V_{GS}\big)_P = V_{IN} - V_{DD} = 0.70 - 0.7\ \text{V} = 0.0\ \text{V} > V_{TP}$ (PMOS is OFF)
Since the PMOS is OFF and the NMOS ON, the output node is connected to ground, so $V_{OUT} = 0.0$.
$V_{DS}\big)_N = V_{OUT} - 0 \approx 0 - 0 = 0\ \text{V} < V_{DSAT}\big)_N$ (NMOS is in the LINEAR region)
$V_{DS}\big)_P = V_{OUT} - V_{DD} \approx 0.0 - 0.7 = -0.7\ \text{V} < V_{DSAT}\big)_P$ (PMOS is in SATURATION)

The NMOS is ON and in the LINEAR region. The PMOS is OFF or we could say that it is in the subthreshold region and in SATURATION.

4) Consider the transistors shown in problem 1), assume $W = 200$ nm, $V_{DD} = 0.7$V, and answer the following two questions.

4a) The gate length for so-called 14 nm technology is actually about 20 nm. The intrinsic speed of a transistor is the time it takes for an electron (or hole) to cross the channel from the source to the drain. Find the device transit time when a CMOS inverter is discharging the output node. (Assume a saturation velocity for electrons of $\upsilon_{satn} = 1.0 \times 10^7$ cm/s and $\upsilon_{satp} = 0.6 \times 10^7$cm/s.

Solution:
The inverter discharges its output capacitor through the NMOS transistor, so it is the NMOS saturation velocity that is relevant here. The transit time is

$$t_t = \frac{L}{\upsilon_{satn}} = \frac{20 \times 10^{-7}}{1 \times 10^7} = 0.2 \times 10^{-12} = 0.2 \text{ psec}$$

$$\boxed{t_t = 0.2 \text{ psec}}$$

Unit 1 Homework SOLUTIONS (continued)

4b) A typical capacitance at a node (the so-called switching capacitance) is 1 femtofarad. Find the time it takes for the CMOS inverter to discharge the output node assuming the transistors technology shown in problem 1).

Solution:
The capacitor discharges through the NMOS. During much of the discharge cycle, the NMOS is in saturation, so the relevant current is the ON-current of the NMOS.

$$\tau = \frac{CV_{DD}}{I_{ON}} = \frac{10^{-15} \times 0.7}{1.1 \times 10^{-3} \times 0.2} = 3.2 \times 10^{-12} = 3.2 \text{ psec}$$

$$\boxed{\tau = 3.2 \text{ psec}}$$

Note: This time is called the "delay metric" – it is a measure of the speed of the circuit. As discussed in the lecture, the delay time of a circuit is usually defined as the time it takes to charge or discharge the capacitor half way, so the delay time of the circuit would be one-half of the above value.

4c) What determines the speed of a CMOS circuit? The intrinsic device speed (i.e. the transit time) or the capacitive charging / discharging time?

Solution:
In this example for which W/L = 10, the capacitor discharging time is much longer than the device transit time. In practice, the NMOS device would transition from SATURATION to LINEAR region during the discharge cycle, so we have overestimated the effective current during the discharge cycle. **In practice, the circuit capacitance charging / discharging times are much more important than the device transit time.**

5) In Lecture 1.5, we discussed an energy band view of N-MOSFETs. A similar discussion explains how P-MOSFETs work in terms of energy band diagrams. Answer the following questions for P-MOSFETs.

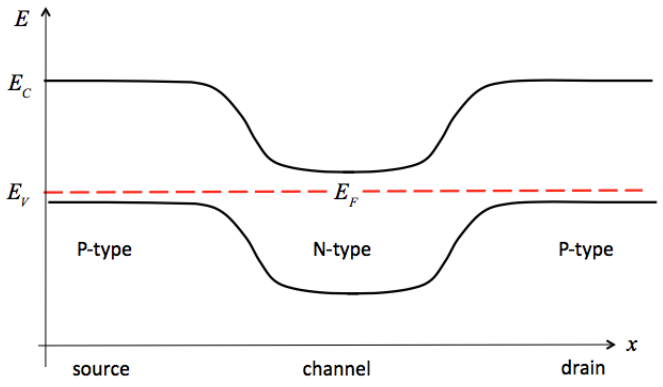
   a) Sketch the equilibrium energy band diagram of a P-MOSFET.
   b) Sketch the energy band diagram in the linear region of operation.
   c) Sketch the energy band diagram in the saturation region of operation.
   d) Sketch the energy band diagram in the off-state with a large (magnitude) drain voltage applied and with no gate voltage applied.

Unit 1 Homework SOLUTIONS (continued)

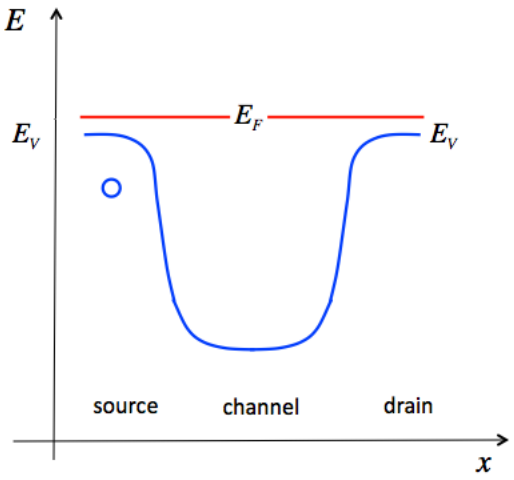
Solutions:

See the energy band diagrams below.

5a) Sketch the equilibrium energy band diagram of a P-MOSFET.



Since we are primarily concerned with how holes in the valence band flow from the source to drain, let's focus on the valence band – as shown below in equilibrium.

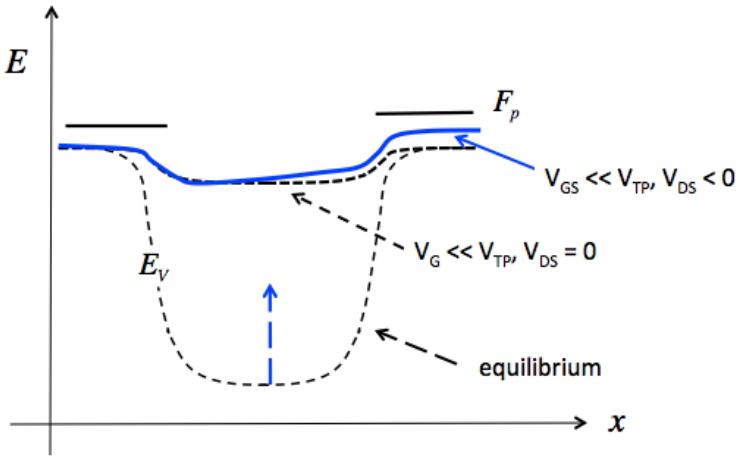


Note that this is an electron energy band diagram. For holes, energy increases downwards.

5b) Sketch the energy band diagram in the linear region of operation.

For a P-MOSFET in the linear region, we apply a gate voltage that is more negative than the (negative) threshold voltage and a small magnitude, negative drain voltage. Negative voltages increase electron energy, so they move the valence band up. In the channel it moves up a lot, and in the drain, it moves up a little.

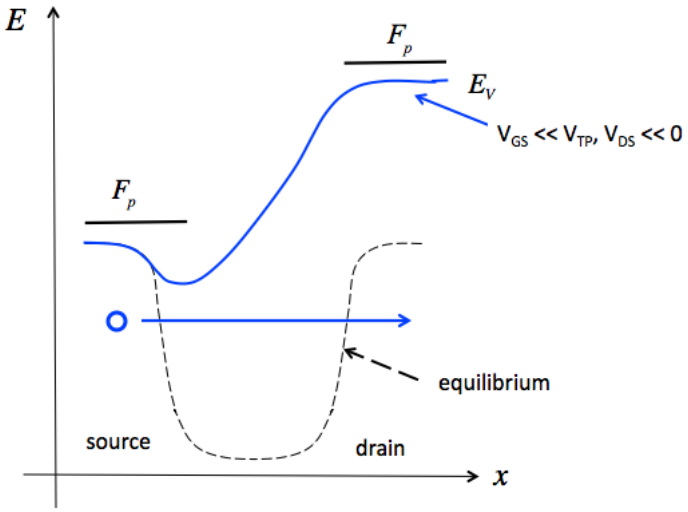
Unit 1 Homework SOLUTIONS (continued)



5c) Sketch the energy band diagram in the saturation region of operation.

$V_{DS} << 0$ - the negative drain voltage increases the valence band energy in the drain.

$V_{GS} << V_{TP} < 0$ - the negative gate voltage increases the valence band energy in the channel (lowers the hole barrier). Holes can hop over their barrier and flow to te drain.

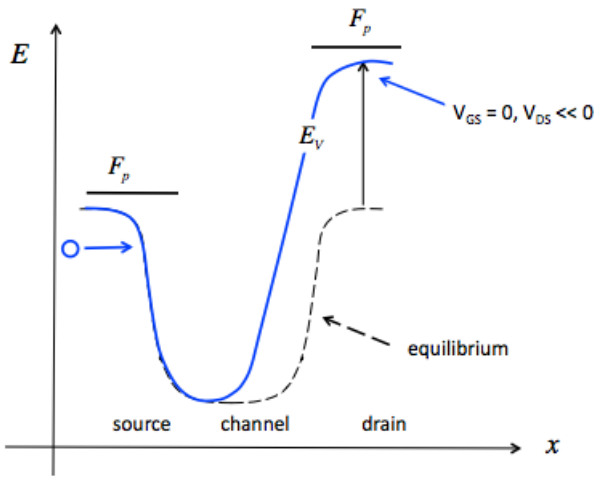


Unit 1 Homework SOLUTIONS (continued)

5d) Sketch the energy band diagram in the off-state with a large (magnitude) drain voltage applied and with no gate voltage applied.

$V_{DS} << 0$ - the negative drain voltage increases the valence band energy in the drain.

$V_{GS} = 0$ - the source to channel barrier for holes is the same as in equilibrium.


E
F_p
F_p
E_V
$V_{GS} = 0, V_{DS} << 0$
equilibrium
source
channel
drain
x