Fundamentals of Nanotransistors
Unit 1 Homework

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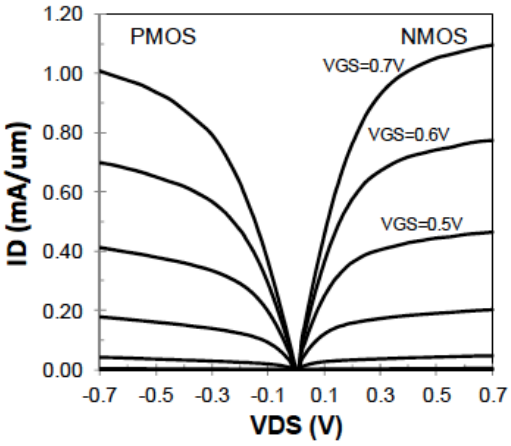
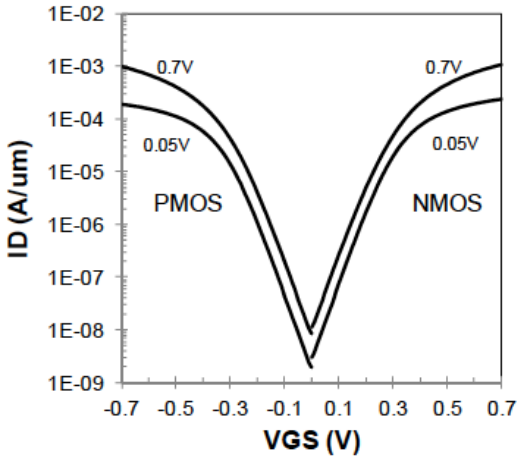
1) The *IV* characteristics of an N-MOSFET for the 14 nm technology node are shown below. Reading from the graphs as carefully as you can, estimate the following key device metrics and other parameters for this device.

   a) threshold voltage assuming that the device is "on" when $I_D = 10^{-5}$ A/μm.
   b) on-current: I_{ON}
   c) off-current: I_{OFF}
   d) subthreshold swing, SS
   e) drain induced barrier lowering: DIBL
   f) total drain to source resistance: R_{TOT} (in the linear region for V_{GS} = 0.7 V)
   g) drain saturation voltage: V_{DSAT} (for V_{GS} = 0.7 V)
   h) output resistance: r_o (in the saturation region for V_{GS} = 0.7 V)
   i) transconductance: g_m (for V_{GS} = 0.7 V, V_{DS} = 0.7 V)

   Be sure to include units for all of your answers.





Source:
S. Natarajan, et al., "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 um2 SRAM cell size," pp. 70-72. Tech. Digest, Intern. Electron Dev. Mtg, Dec. 2014.

Unit 1 Homework (continued)

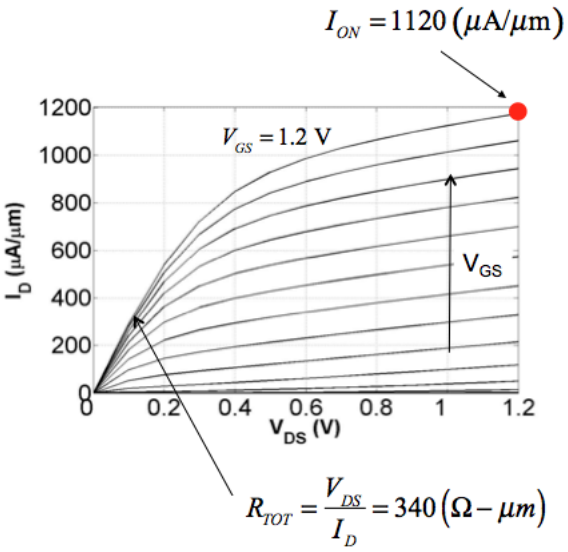
2) Measured *IV* data for an N-MOSFET are shown below. Relevant parameters for this MOSFET are:

T = 300 K
Oxide thickness: $x_0 = 2.2$ nm Relative dielectric constant: $\kappa_{ox} = 4$
Power supply voltage: $V_{DD} = 1.2$ V Series resistances: $R_{S0} = R_{D0} = 80\,\Omega - \mu$m
Channel length = 85 nm Channel width, $W = 10^{-4}$ cm.
$V_{TLIN} = 0.28$ V.

Answer the following questions.

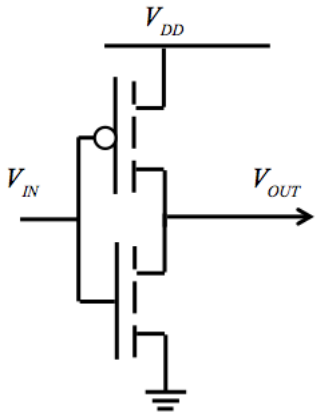
2a) What is the resistance of the intrinsic channel for $V_{GS} = 1.2$ V?

2b) Estimate the mobility of electrons in the channel at $V_{GS} = 1.2$ V?



Unit 1 Homework (continued)

3) A CMOS inverter is shown below. Assume that the NMOS and PMOS transistors in this circuit are the same ones shown in problem 1). Assume that $V_{DD} = 0.7$ V. For each of the input voltages list below, determine the region of operation for each of the transistors.
   a) $V_{IN} = 0.0$ V
   b) $V_{IN} = 0.15$V
   c) $V_{IN} = 0.35$ V
   d) $V_{IN} = 0.70$ V



4) Consider the transistors shown in problem 1), assume $W = 200$ nm, $V_{DD} = 0.7$V, and answer the following two questions.

   4a) The gate length for so-called 14 nm technology is actually about 20 nm. The intrinsic speed of a transistor is the time it takes for an electron (or hole) to cross the channel from the source to the drain. Find the device transit time when a CMOS inverter is discharging the output node. (Assume a saturation velocity for electrons of $\upsilon_{satn} = 1.0 \times 10^7$ cm/s and $\upsilon_{satp} = 0.6 \times 10^7$cm/s.

   4b) A typical capacitance at a node (the so-called switching capacitance) is 1 femtofarad. Find the time it takes for the CMOS inverter to discharge the output node assuming the transistors technology shown in problem 1).

   4c) What determines the speed of a CMOS circuit? The intrinsic device speed (i.e. the transit time) or the capacitive charging / discharging time?

Unit 1 Homework (continued)

5) In Lecture 1.5, we discussed an energy band view of N-MOSFETs. A similar discussion explains how P-MOSFETs work in terms of energy band diagrams. Answer the following questions for P-MOSFETs.

   a) Sketch the equilibrium energy band diagram of a P-MOSFET.
   b) Sketch the energy band diagram in the linear region of operation.
   c) Sketch the energy band diagram in the saturation region of operation.
   d) Sketch the energy band diagram in the off-state with a large (magnitude) drain voltage applied and with no gate voltage applied.